

HIROSHIMA UNIVERSITY

MASTER'S THESIS

The Detector Control System for the Muon Forward Tracker at ALICE

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HIROSHIMA UNIVERSITY

*Abstract*Department of Physical Science
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Master of Science

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The Quark Gluon Plasma (QGP) is a new state of matter in the extremely high temperature and density region where quarks and gluons are deconfined. In the ALICE experiment with LHC at CERN, the experimental study of QGP with the world's highest energy heavy ion collisions has been conducted. A new detector, the Muon Forward Tracker (MFT), will be operated in ALICE from the LHC RUN-3 (2022-) after the current LHC long-shutdown. MFT is an up-to-date silicon pixel detector which achieves high spatial resolution ($\sim 10 \mu\text{m}$) and low material budget ($X/X_0 = 0.55\%$ for each disk). Before installing MFT, the multiple scattering in a hadron absorber in front of the muon spectrometers worsen the spatial resolution near the vertex. The MFT is placed between the hadron absorber and collision vertex for more precise measurements.

This thesis describes the development and implementation of the detector control system (DCS) to operate MFT remotely. In the LHC-Run3, a new computing system is employed for continuous data readout with 50 kHz in Pb-Pb collisions. The maximum raw data size reaches to 3.4 TB/s. Therefore, data reduction is needed at the same time with data transfer. The DCS data share the data flow with physics data to be used for data reduction. DCS must be re-designed to match the new computing scheme. MFT is composed of 936 silicon chips on 5 disks and 2 power supply units. The low voltage channels and 80 readout unit boards are also necessary for MFT. In order to control these enormous channels, comprehensive control is essential. Furthermore, it is necessary to construct a safety system that automatically detects and responds to an abnormal state. The DCS of MFT consists of various elements, such as a finite state machine (FSM) and GUIs for operators. The newly created FSM has a hierarchical structure based on the hardware structure. It simplifies and automates controls, and realize easy monitoring. For example, when the temperature exceeds the threshold, the corresponding low voltage channel is turned off. Operation tests for these functions of the DCS were conducted in parallel with the development. A part of FSM and GUIs were first tested with a test bench built at Hiroshima University. For one year from October 2019, the whole MFT was tested on the ground at CERN. The operation of the power supply system and the readout unit boards were tested there. Finally, from November 2020, the MFT was installed in the ALICE detector in a cavern. The final commissioning is ongoing, and the control of some devices is established.

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List of Abbreviations

ALF	ALICE Low-level Front-end
ALPIDE	ALICE Pixel Detector
ANA	ANALog
ASIC	Application Specific Integrated Target
BB	Back Bias
CAEN EASY	CAEN Embedded Assembly SYstem
CGC	Color GlassCondensate
CRU	Common Readout Unit
DCS	Detector Control System
DSS	Dtector Safety System
DEN	Device Editor Navigator
DIG	DIGital
DIM	Distributed Iinformation Management system
DPE	Data Point Element
DPT	Data Point Type
DP	Data Point
EPN	Event Processor Node
FIT	Fast Interaction Trigger
FLP	First Level Processor
FPC	Flexible Printed Circuit
FPGA	Field Programmable Gate Array
FRED	FRont End Device
GBT-SCA	GBT Slow Control Adopter
GBT	GigaBit Transceiver
GEM	Gas Electron Multiplier
Gedi	Graphical EDItor
ITS	Inner Tracking System
JCOP	Joint COntrol Project
LHC	Large Hadron Collider
LS2	Long Shutdown 2
LV	Low Voltage
LVPS	Low Voltage Power Supply
MAPI	Message API
MFT	Muon Forward Tracker
MWPC	Multi Wire Proportional Chambers
O²	Online Offline computing system
PLC	Programmable Logic Controllers
PSU	Power Supply Unit
PS	Proton Synchrotron
QCD	Quantum ChromoDynamics
QGP	Quark Gluon Plasma
RHIC	Relativistic Heavy Ion Collider
SCADA	Supervisory Control And Data Aquisition

SCA	Slow Control Adopter
SPS	Super Proton Synchrotron
SWT	Single Word Transaction
TOF	Time Of Flight
TPC	Time Projection Chamber
TRD	Trantision Radiation Detector
TTS	Timing Trigger System
WinCC OA	WinCC Open Architecture

Chapter 1

Introduction

1.1 Quark Gluon Plasma (QGP)

According to the standard model that is generally agreed upon today, all substances in our universe consist of 17 kinds of elementary particles. They interact with four kinds of fundamental forces. They are gravity, the weak force, electromagnetic force, and the strong force. A quark is a kind of elementary particle, and it interacts by the strong force. It consists of the fundamental elements of matter. For example, a proton is composed of two up quarks, and one down quark, and a neutron is composed of one up quark and two down quarks. Quantum Chromodynamics (QCD) describes the strong interaction between quarks and gluons. In normal conditions, quarks are confined in hadrons such as baryon and meson, and therefore they can not be observed by themselves. This characteristic property of QCD is called quark confinement. According to the QCD, static potential between quark and anti-quark follows Eq. 1.1 and Fig. 1.1. These results indicate that the attractive force by strong force increases as the distance between quarks. If the distance between quarks reaches a certain point, it is more favorable to create a quark and anti-quark pairs for each of them. Thus, a single quark can never be isolated.

$$V(r) = V_0 - \frac{\alpha}{r} = \sigma r \quad (1.1)$$

Quarks and gluons are deconfined in a extremely high temperature and densities. It is called a quark-gluon plasma (QGP). Due to an increase in temperature and density, a phase transition occurs, and quarks and gluons move freely in the medium like plasma. Figure 1.2 is the schematic phase diagram of QCD. The vertical axis represents temperature, and the horizontal axis represents chemical potential. The region of high temperature with low net baryon density is achieved by high-energy particle collisions. It is calculated by lattice QCD, and it is predicted that the hadronic phase transitions to the QGP at the critical temperature $T_C \sim 150$ MeV. The phase transition around $\mu = 0$ is a crossover, which is the state quantity gradually changes [28]. The QGP is also vital to investigate the history of the universe. Immediately after the big bang ($\sim 10^{-10}$ μ), the temperature was extremely high, and the universe was filled with the QGP. Afterward, it cooled due to expansion, and it transitioned to the hadron phase. Therefore, the phase transition of QGP to hadron leads to the origin of matter.

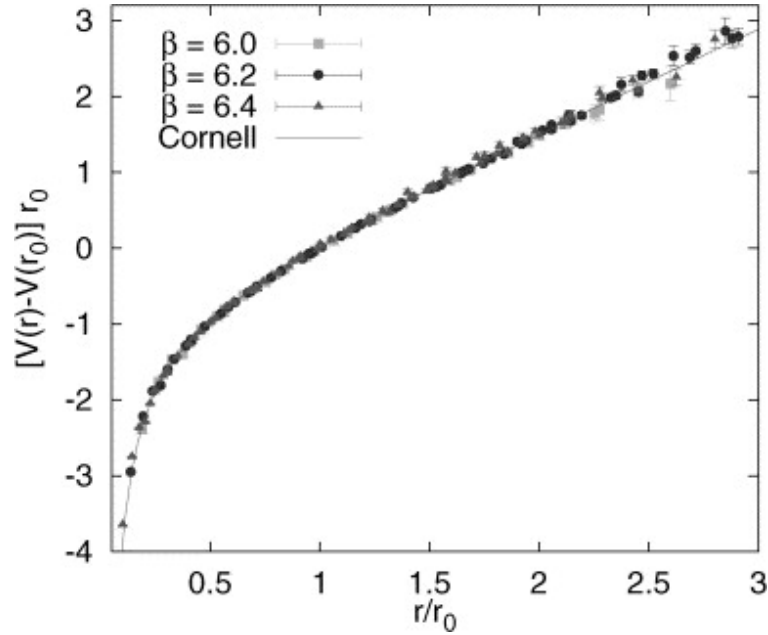


FIGURE 1.1: QCD Potential [11]

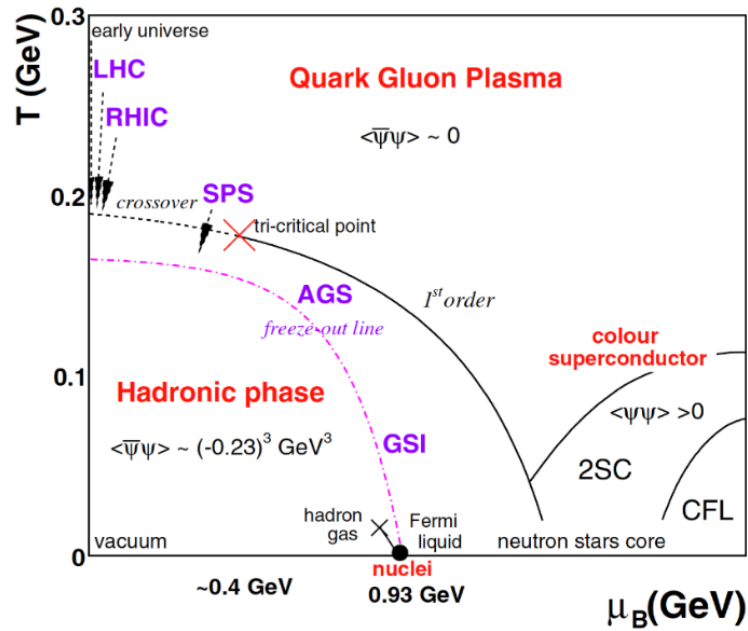


FIGURE 1.2: The schematic phase diagram of QCD [15]

1.2 Heavy Ion Collision

1.2.1 History and Achievements

High energy heavy ion collisions by large accelerators are currently the most powerful tool to generate QGP experimentally [22]. Since the theory calculations implied the existence of QGP in the 1970s, several experiments aimed at generating QGP have been conducted. Since the mid-1980s, AGS at BNL and SPS at CERN started to obtain the evidence of QGP formation. They had results that could be

an indication of QGP formation, but no definitive evidence was obtained [9]. In the 2000s, the larger accelerators, RHIC (Relativistic Heavy Ion Collider) and LHC (Large Hadron Collider) has started. LHC can produce the largest collision energy in the world ($\sqrt{s}_{NN} = 5.02$ TeV in Pb-Pb collision). Figure 1.3 shows the transition of the available center of mass energy. RHIC and LHC found many signatures of QGP. Today, the main topic is to study the property of QGP produced in heavy ion collision. It can feature the new property of QCD that is difficult to predict from theory.

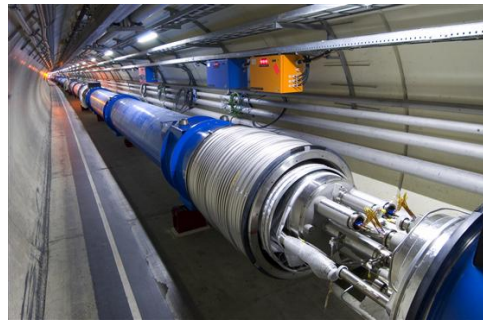
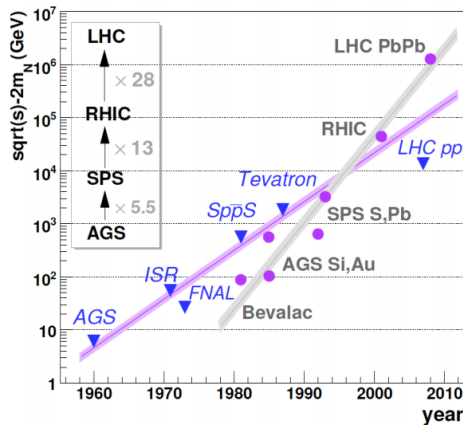


FIGURE 1.3:
Available center-
of-mass energy
[15]

FIGURE 1.4: The
beam pipe of LHC
[37]

1.2.2 Time Evolution

Heavy ion collision experiences several phases. The results are discussed by adopting the theoretical models for each phases. This will help to improve our understanding of the time evolution of QGP. Figure 1.5 shows the time evolution of a high energy heavy ion collision. Heavy ions are accelerated to near the speed of light. It looks like a disk from a laboratory system because of the Lorentz contraction. In high energy by LHC and RHIC, gluons with small momentum scatter and accumulate the energy at the vertex ($\epsilon > 1\text{GeV}/\text{fm}^3$). QGP is generated when reaching thermal equilibrium. It expands and cools down over time. The relativistic hydrodynamics describe time evolution. When the temperature becomes below the phase transition temperature ($T_C \sim 150$ MeV), the phase transitions from the QGP to the hadron phase ($\tau \sim 10$ fm/c). After that, the inelastic scatterings stop and the particle ratios are fixed (chemical freezeout). Subsequently, the elastic scatterings stop, and the momentum of particles is fixed (kinetic freezeout). Since inelastic scatterings occur between the generated particles, transport calculation describes the final state particles until kinetic freezeout. Finally, final state particles fly to the detectors.

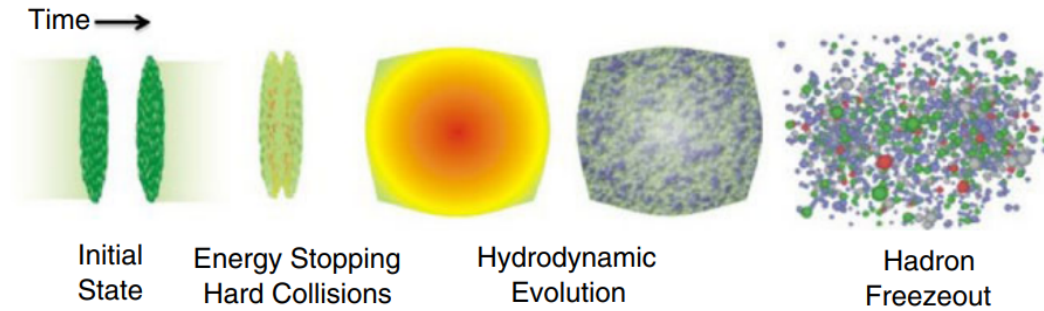


FIGURE 1.5: The time evolution of a high energy heavy ion collision [34]

1.3 ALICE Experiment

1.3.1 Overview

ALICE (A Large Ion Collider Experiment) is one of the major LHC experiment. LHC is the largest circular accelerator in the world located at CERN. Its circumference is 27 km, and it is in a depth of 50 to 100 meters underground. LHC started proton-proton collisions at $\sqrt{s} = 900$ GeV in 2009. At present, it can collide protons up to $\sqrt{s} = 14$ TeV and leads up to $\sqrt{s_{NN}} = 5.5$ TeV. The CERN accelerator complex is shown in Figure 1.6. Particles are accelerated in stages using multiple accelerators. In the beginning, protons are accelerated at LINAC2 (ions at LINAC3) linearly and injected to PS (Proton Synchrotron). After being fully accelerated, it is sent to the larger accelerator SPS (Super Proton SYNchrotron). Finally, the SPS delivers the accelerated particles to the largest accelerator LHC and generates collisions at the LHC experiments.

ALICE is the only experiment specializing in studying the properties of QGP. Hiroshima University, the University of Tokyo, the University of Tsukuba, Nara Woman's University, and Nagasaki Institute of Applied Science join the ALICE experiment from Japan.

1.3.2 Apparatus

Figure 1.7 is the appearance of the ALICE detector. It is the complex of several detectors and is designed to measure the particles in a wide range of particle and momentum. The detector is 16 meters tall, 16 meters wide, and 26 meters long, and the total weight is about 10000 tons [23]. The central part is called the central barrel. It is comprised of sub-detectors for tracking and momentum measurement of charged particles. The central-barrel detectors are in a magnetic field of 0.5 T. They are essential for charged particle identification and momentum measurement. Global detectors are used for collision event selection. They count the particles produced by collision and are used to determine the centrality, event plane and trigger. In the forward region, detectors to measure muons are installed. It covers the pseudorapidity region $-4 < \eta < -2.5$. Hadron absorber is installed between the five pad chambers and the vertex. With the five pad chambers and dipole magnet installed by the third pad chamber, it measures the track and momentum.

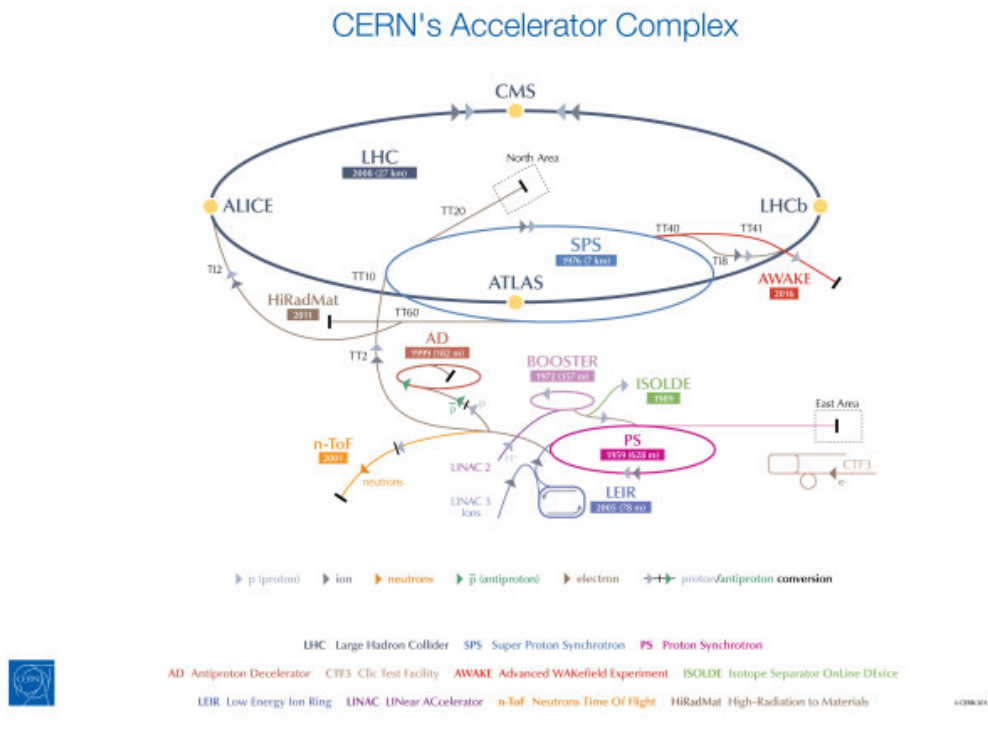


FIGURE 1.6: CERN's Accelerator Complex [25]

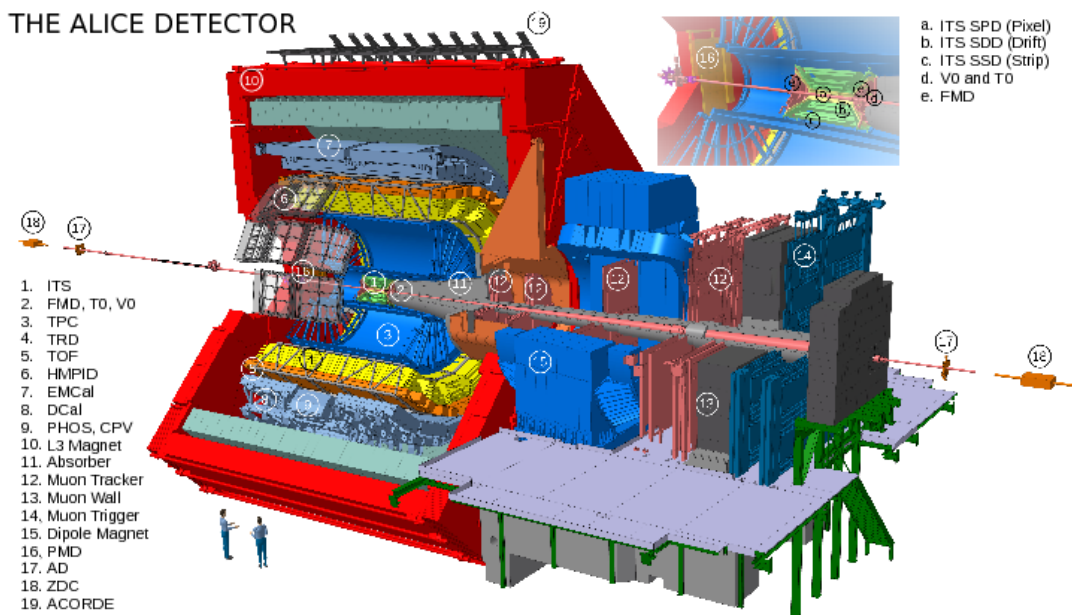


FIGURE 1.7: The ALICE detector [35]

1.3.3 Upgrade Program

LHC is currently in the phase of the Long shutdown (LS2). Under the current schedule, the LHC will restart for RUN-3 in May 2022. After LS2, the LHC beam interaction rate will increase up to 50 kHz in Pb-Pb collisions, and the beam luminosity to

$L = 6 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1}$. ALICE will upgrade the current detectors for more precious measurement. The readout system is also improved, and it will acquire all collisions at 50 kHz in Pb-Pb collisions continuously. It increases by a factor of 100 for the minimum bias data compared to the previous Run. The specific improvement of each detector and readout system is shown below [10].

ITS The current Inner Tracking System (ITS) will be entirely replaced by the new one to improve the vertexing and tracking performance.

MFT Muon Forward Tracker (MFT) is a new silicon detector to improve the muon measurement. It is installed between vertex and hadron absorber. Details are given in the Sec. 1.5.

TPC The current Time Projection Chamber (TPC) adopts multi-wire proportional chambers (MWPC), and it will be replaced by the Gas Electron Multiplier (GEM). GEM system at ALICE will be able to read out at a collision rate of 50 kHz continuously.

FIT The Fast Interaction Trigger (FIT) is the new detector for the trigger placed at the forward region. It consists of two arrays of Cherenkov radiators.

Readout electronics of several detectors The readout electronics of Muon spectrometer, Transition Radiation Detector (TRD), and the Time Of Flight (TOF) will be improved to cope with the new collision rate.

Online-Offline Computing system Online-Offline Computing system (O^2) is a new computing system to improve the data processing. Details are given in the Sec. 1.4.

1.4 Online-Offline Computing system

From LHC RUN-3, which starts in 2022, ALICE focuses on measuring rare and difficult-to-measure events. The LHC will conduct Pb-Pb collisions at a rate of 50 kHz and pp at 200 kHz. The target integrated luminosity is 13 nb^{-1} in Pb-Pb collisions, 10 nb^{-1} at the full magnetic field in the solenoid, and 3 nb^{-1} with a reduced field of $B = 0.2 \text{ T}$. Data volume of heavy ion collision event will be 3.4 TB/s. This high statistic data set will significantly improve the measurement of rare probes, such as heavy quarks.

ALICE plans continuous readout and more precise measurements. To process a huge amount of data, O^2 is proposed as an alternative to the current computing system. O^2 performs detector calibration, track reconstruction and background rejection in parallel with the data collection. Only compressed data are transferred to the storage. New computing devices and software are used for it [12]. Figure 1.8 shows the hardware implementation and data flow of O^2 . First Level Processor (FLP) and Event Processing Node (EPN) are computers for data reduction in O^2 . FLP conducts calibration and masking of physics data. Useless data such as back ground data are removed here. It collects physics data and DCS data in a same data flow. DCS data, i.e., whether the detector is active and what configuration it is in, is used for data reduction. EPN collects only physics data, and conducts online tracking and reconstruction. Those data replace the raw data, and be sent to the storage.

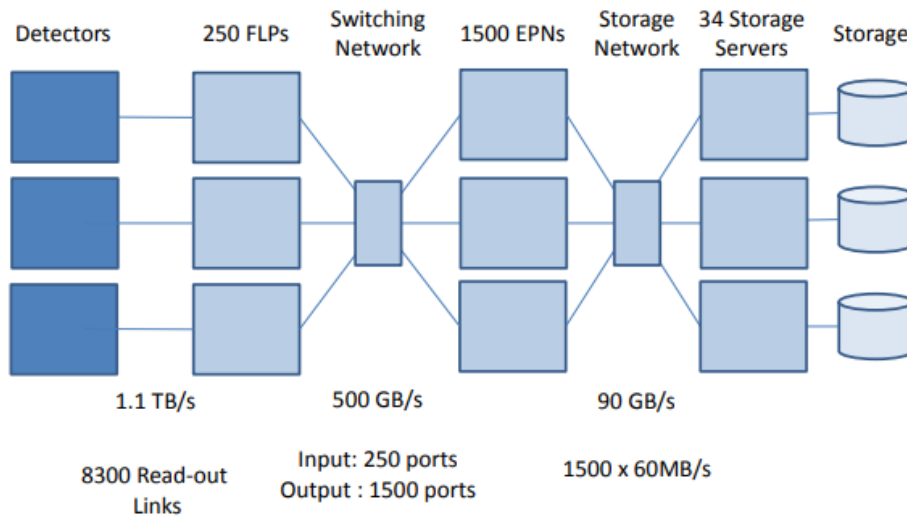


FIGURE 1.8: Hardware implementation and data flow of O^2 [12]

1.5 Muon Forward Tracker

1.5.1 Overview

The second generation leptons, muons, are an effective tool to study QGP. Since leptons do not interact with the strong force, it preserves the information at the time of its generation. Heavy flavor hadrons and low mass vector mesons, that are important for QGP study, decay into lepton. Compared to the electron measurements, the muon measurements have less background and they are easy to be sorted out from a hadron absorber due to its long lifetime. MFT is the new detector to improve the muon measurements. It is installed in front of the hadron absorber. Up-to-date silicon pixel chips are used to achieve high spatial resolution.

1.5.2 Current setup and upgrade strategy

In the ALICE experiment, electrons are detected in the central region, and muons are in the forward region. Figure 1.9 shows the schematic of the current setup for the muon measurement and the installation location of MFT. The hadron absorber made of concrete, iron, and carbon absorbs the particle except for muon. Muons are detected with five pad chambers behind the absorber. Electromagnets are placed beside the third tracker, and muon momentum can be determined from its curvature. Behind the five trackers, iron wall, and two trigger detectors are placed to trigger muon events. This muon spectrometer provided a much significant result so far. However, the vertex and invariant mass resolution are limited due to the multiple scattering in the absorber, particularly at low transverse momentum (pT). Pion, kaon, and their semi-muonic decay products also smear out the resolution. The lack of information near the vertex prevents the identification of J/ψ from B-hadron and separate measurement of charm and bottom.

In order to overcome this limitation, the new silicon pixel detector named MFT (Muon Forward Tracker) is installed between the collisions vertex and the hadron

absorber [8]. It covers the forward region ($-2.45 < \eta < -3.6$), matching the muon spectrometer acceptance. MFT tracks all the charged particles before the absorber. Then, the tracks by the MFT and the muon spectrometer are connected. MFT improves the resolution of vertex and momentum to overcome the problem those are mentioned above.

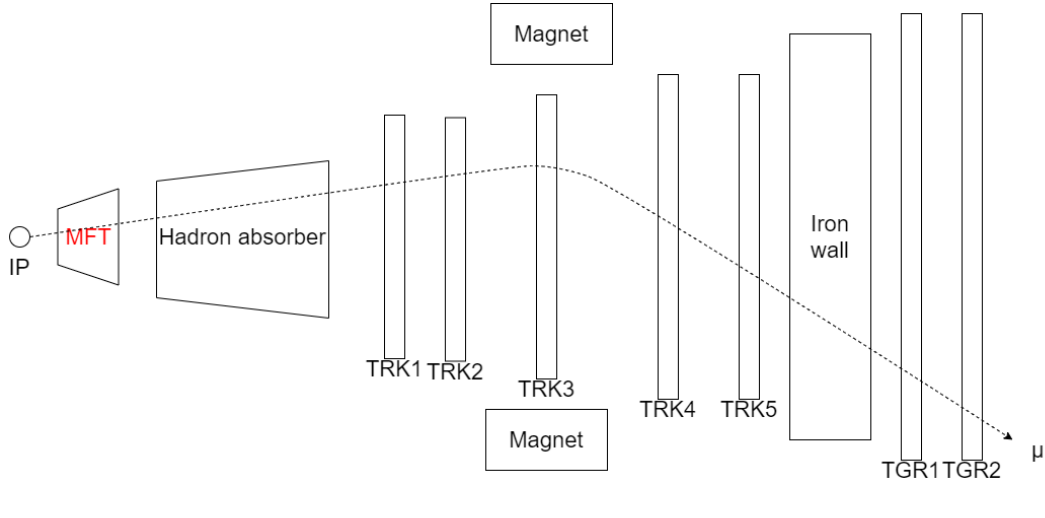


FIGURE 1.9: Schematic of Muon Spectrometer and MFT

1.5.3 Physics Upgrade

Heavy Flavor In high energy collisions, heavy quarks, namely charm and bottom quarks, are generated. These quarks have a larger mass than a typical QGP temperature. So they are generated at initial collisions and they are hardly generated thermally. Therefore, their production cross sections and initial momentum distributions can be studied with pp collisions. Heavy quarks lose their energy in QGP with Brownian motion. Comparing the experimental result with hydrodynamic model calculation using the relativistic Langevin equation, the diffusion coefficient of QGP can be determined. Thus, heavy quark measurements are essential to study QGP property.

It is promising to make better measurements of muons from heavy flavour hadrons with MFT. Heavy flavor forms D meson (charm and light flavor quark), and B meson (bottom and light flavor quark) and they emit muons by decay. They are identified by measuring the decay point taking advantage of D meson and B meson's different lifetime. In the measurement in RUN-2, it had been impossible to distinguish them. In the RUN-3, MFT allows for accurate measurement of muon decay points. Therefore, they can be identified separately down to $p_T = 0$ GeV/c. Figure 1.10 shows the achievable measurements of R_{AA}^B/R_{AA}^D with expected uncertainties. R_{AA} is nuclear modification factor (Eq. 1.2). It is a factor to compare the particle yields between A-A collisions and p-p collisions. Particle yields is normalized by the number of nucleon-nucleon collisions N_{coll} . The uncertainty using the MFT is compared with the ones using the new ITS at central rapidity.

$$R_{AA}(p_T) = \frac{dN^{AA}/dp_T}{\langle N_{coll} \rangle dN^{PP}/dp_T} \quad (1.2)$$

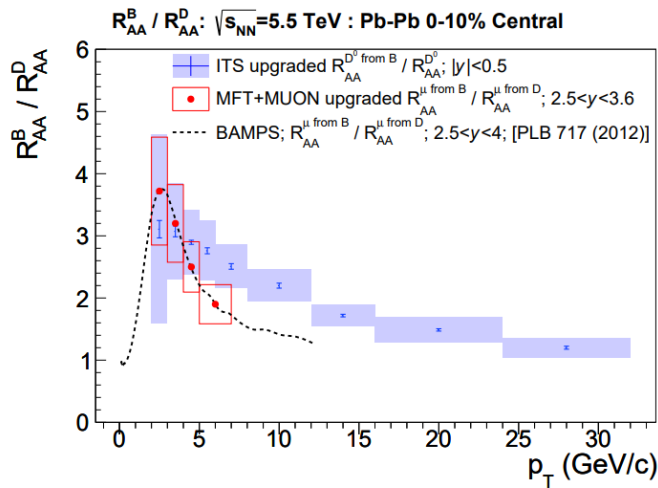


FIGURE 1.10: Ratio of the nuclear modification factors of open charm and beauty [8]

Quarkonium Quarkonium is heavy quark and anti-quark bound states such as J/ψ of $c\bar{c}$ and Y (1S, 2S, 3S) of $b\bar{b}$. In the high energy particle collision, heavy quarks such as charm and bottom are produced only by initial collision, and part of them forms quarkonium. When QGP is formed, the quarks and gluons in the medium prevent the interaction between $c\bar{c}$ and $b\bar{b}$. As a result, quarkonium yield is suppressed compared to the collisions without QGP formation. The suppression of quarkonia can be one of the strong evidences of QGP formation [26]. The dissociation temperature of J/ψ is 1.5 to 2 times higher than the QGP phase transition temperature (~ 150 MeV) [31]. The binding energy and system radius differ depending on resonance state, and they result in different dissociation temperatures. A temperature of the medium can be evaluated by measuring the quarkonia yield suppression systematically. Figure 1.12 compares Y (1S, 2S, 3S) yields in Pb-Pb collision measured at CMS experiment. Binding energy of three state of Y , Y (1S, 2S, 3S) are higher in Y (3S) $<$ Y (2S) $<$ Y (1S). The amount of yield suppression is expected to be Y (1S) $<$ Y (2S) $<$ Y (3S).

Quarkonia have a dimuon decay channel. Then they can be identified by invariant mass reconstruction with measured dimuons. In the LHC RUN-2, inclusive J/ψ and ψ' are measured by the muon spectrometer. Inclusive J/ψ includes J/ψ from B-hadron, and it was impossible to separate them from J/ψ generated by initial collisions (noted as direct J/ψ). Precise measurement of a decay point by MFT enables distinguishing prompt J/ψ and B-decayed J/ψ thanks to their lifetime difference. Systematic measurements of quarkonia lead to the study of their dissociation and recombination through QGP. Figure 1.11 shows the decay length distribution of prompt J/ψ and J/ψ from B-hadron. B-decayed J/ψ can be removed by utilizing a decay length.

1.5.4 Hardware Component

Figure 1.13 shows the entire MFT and its component. It is divided into two half detectors, up and bottom. Each half detector is composed of five disks. Each disk has two detection planes on each side. A half plane is divided into four zones. A

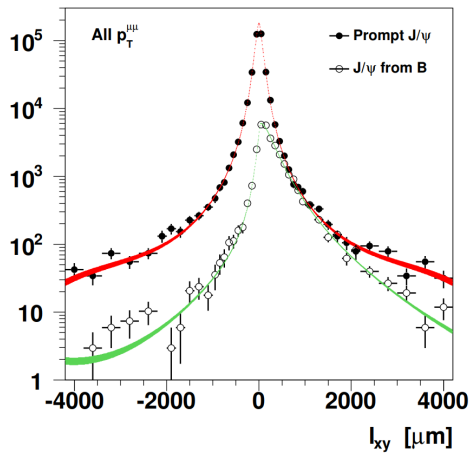


FIGURE 1.11: Pseudo-proper decay length distribution of prompt J/ψ and J/ψ from b-hadron [8]

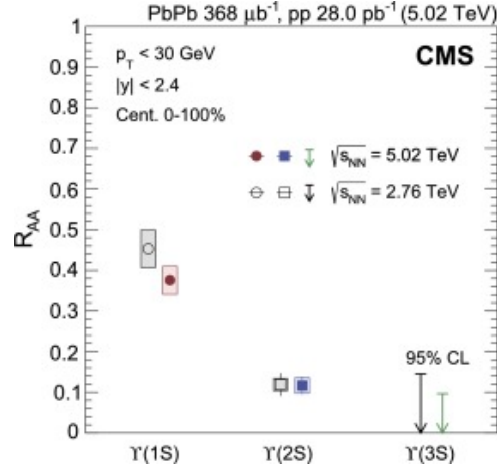


FIGURE 1.12: Nuclear modification factor of Y measured in Pb-Pb Collision [16]

power is supplied for each zone. In this paper, MFT components are expressed as H#D#F#Z#. Each # is the number to address the part of MFT. H# express the Half MFT, 0 is the bottom part, and 1 is the top part. D# is the disk number (0-4), F# is the face number (0,1), and Z# is the zone number (0-3).

A CMOS monolithic pixel sensor technology is adopted for sensors, called ALPIDEs (ALICE Pixel DEtector) [24]. The readout electronics of the sensor are integrated into the same substrate. It allows for thinner, higher resolution silicon chips and reduces power consumption. Its pixel pitch is $25\mu\text{m}$ and the spatial resolution is $5\mu\text{m}$. The material budget is $X/X_0 = 0.55\%$ for each disk. MFT has 936 ALPIDEs in total to detect charged particles. ALPIDEs are integrated on the Flexible Printed Circuit (FPC) called a ladder. Each ladder has 2 to 5 ALPIDEs (Fig. 1.14).

1.6 ALICE Detector Control System for LHC RUN-3

1.6.1 The Detector Control System for ALICE

The detector control system (DCS) is a system to operate each sub-detector from the operators. The ALICE detector is located at about 70 meters underground, and it cannot be operated directly by hand during experiment due to radiation. Therefore, detectors are monitored and controlled remotely from the ALICE control room at LHC Point2 (P2) on the ground. Additionally, since detectors are composed of plenty of channels, comprehensive control by DCS is indispensable. It also acts as a safety interlock that automatically stops operation when a device is in an abnormal state such as too high temperature, ensuring stable operation.

1.6.2 DCS upgrade for LHC RUN-3

From the LHC RUN-3, the detector control system at ALICE will be renewed to correspond to O^2 , a new computing system for data process. The DCS data, such

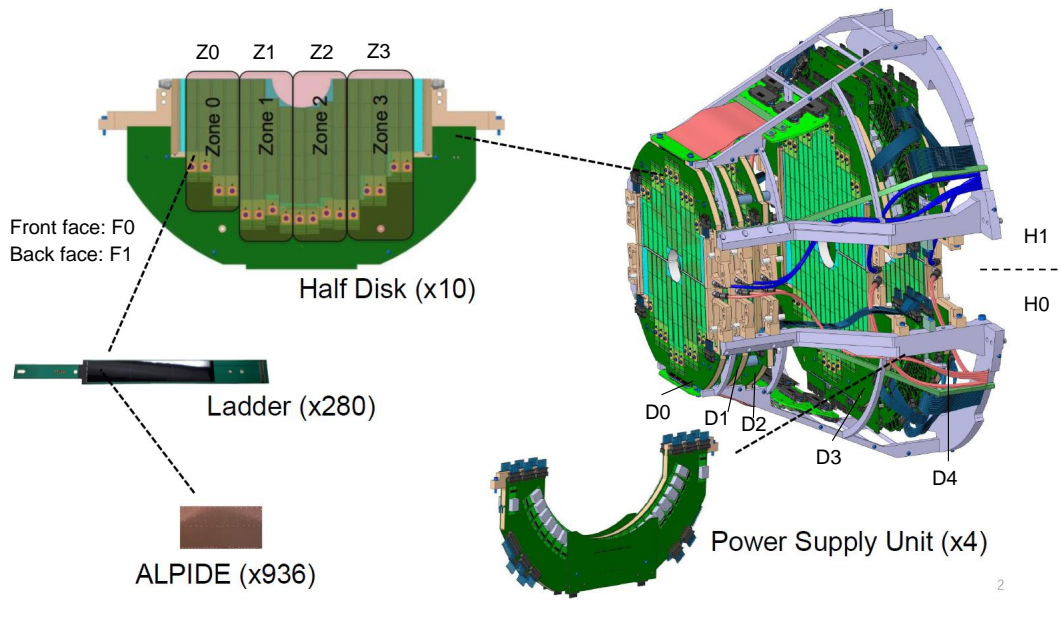


FIGURE 1.13: MFT Component [8]

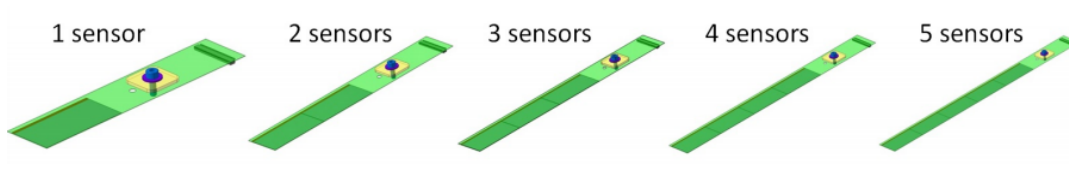


FIGURE 1.14: The 5 types of MFT ladders [12]

as calibration status, is used to reduce physics data. Therefore, physics data and DCS data are transferred through common data flow. Figure 1.15 is the data flow at ALICE RUN-3 in Pb-Pb collisions. Raw physics data are processed at a rate of 3.4 TB/s. FLP hosts a Common Readout Unit (CRU) as an interface to FEE, and CRUs communicate via optical cables. The Giga-Bit Transceiver (GBT) technology developed by CERN for high-speed data transmission is applied for data links between FEE and CRU. FLP divides physics data and DCS data. Reduced physics data are transferred to EPN at a rate of 500 GB/s. It reduces the data, by calibration and masking of physics data on FLPs, and online tracking and reconstruction on EPNs. Finally, data are transferred to the storage at a rate of 90 GB/s. DCS data separated by FLP is sent to DCS-specific software [14]. More specific data flows, and devices are described in Sec. 2.1.

1.7 Physics motivation of this thesis

1.7.1 QGP formation in small system

It is no doubt that QGP is formed in high-energy heavy ion collisions. Surprisingly in recent years, the study to suggest the possibility of QGP formation in small collision system such as proton + proton collisions and proton + nuclear collisions has been reported. For example, Ref. [7] and Ref. [20] reported the medium's collective movement in high multiplicity events. It is regarded as the signature of QGP.

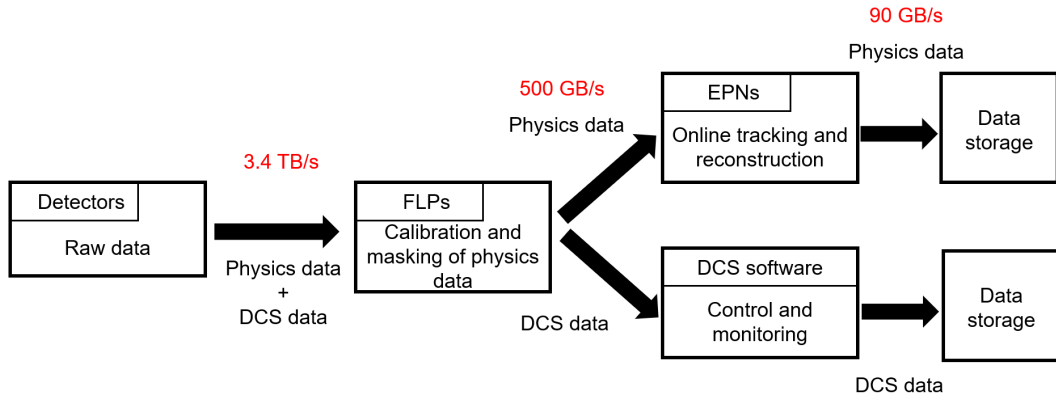


FIGURE 1.15: Physics and DCS data flow at ALICE

Figure 1.16 shows the number of two particles plotted according to the difference in pseudo-rapidity and azimuthal direction measured in pp collisions at LHC. The figure on the left is for high multiplicity, and the figure on the right is for low multiplicity. In high multiplicity, the ridge is observed where the azimuthal difference is 0. It can be interpreted as an effect of collective motion [19]. Another signature for QGP is shown in Fig. 1.17. When QGP is formed, strange quarks are also produced in parton reactions in addition to hadron reactions. Thus, hadrons containing strangeness appear to be increasing. This figure shows that the relative yields of strange hadrons against π increase with the charged particle multiplicity. However, the result showing the collective motion can be described only by the initial effect due to quantum fluctuations. Therefore, QGP formation in a small system is still controversial. More high multiplicity data are needed to conclude this proposition.

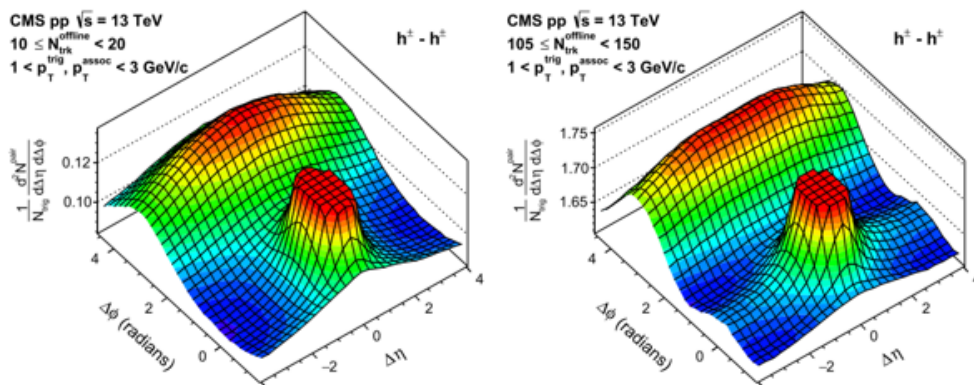


FIGURE 1.16: The 2D particle correlation functions for inclusive charged particles [19]

1.7.2 Methods to study QGP in small system

I am very interested in QGP formation in the small system and would like to study it in LHC RUN-3. I am participating in the ALICE experiment and planning to measure quarkonia (J/ψ) yield systematically via dimuon in high-multiplicity proton-proton collisions at LHC RUN-3 starting in 2022. Quarkonia dissociate in the QGP

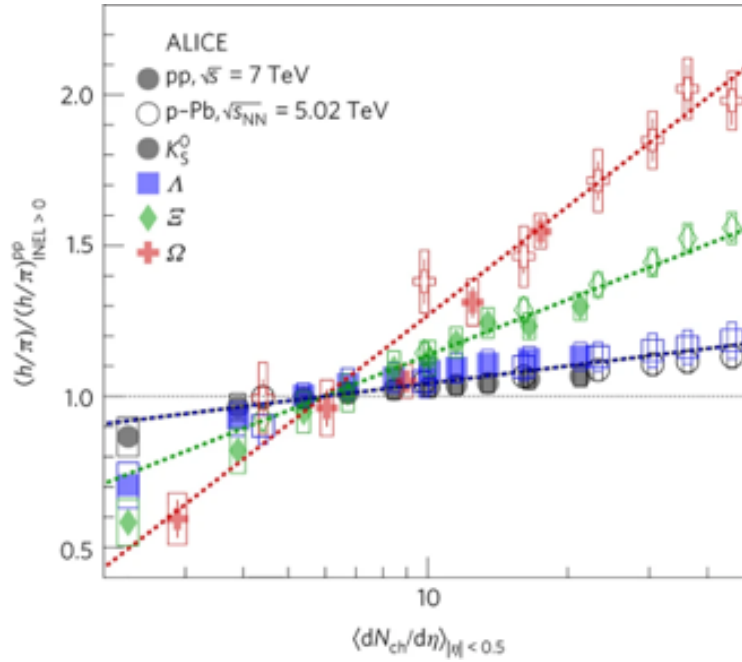


FIGURE 1.17: Particle yield ratios to pion normalized to the values measured in the inclusive INEL > 0 p-p sample [29]

due to color Debye screening, and its yield suppression is the signature for QGP formation. If the yield suppression is measured and the medium is above the QGP phase transition temperature (about 150 MeV), it will be the direct evidence of QGP formation. Therefore, an initial state of the collisions can be defined clearly from the p-p collisions. Thus, it is an excellent probe to investigate the QGP formation.

The high statistical data with O^2 and MFT expected in RUN-3 will enable high precision quarkonium measurements to study QGP formation in a small system. Since there are few high multiplicity events that may be able to form QGP, the increase of data by O^2 is indispensable. Regarding the quarkonium measurement, the identification of direct J/ψ and J/ψ from B hadron is a significant contributor to precise measurement.

1.8 Purposes of This thesis

To study the QGP formation in small systems via quarkonium measurements, I contribute to the MFT installation and operation by developing the new DCS for MFT adopted for O^2 during LS2. I develop and implement MFT DCS, and guarantee a safe and comprehensive operation.

Chapter 2

Detector Control System for MFT

2.1 Architecture of the ALICE DCS

Architecture of the ALICE DCS has been redesigned to cope with the LHC RUN-3. The hardware and software dedicated to new ALICE DCS is prepared to build the system. A detailed description of hardware and software for DCS is shown below.

WinCC Open Architecture (WinCC OA) WinCC OA is a Supervisory Control And Data Acquisition (SCADA) produced by Siemens [33]. SCADA monitors and controls the devices used for the experiment. WinCC OA has been used at four experiments currently being conducted at LHC. WinCC OA monitors all devices, and if the device's output values show abnormal states it will automatically remedy the issue or alert operators. It is also possible to build a system composed of multiple WinCC OA projects running on multiple computers, called distributed projects.

WinCC OA manages data from devices using DPs (Data Point), a kind of data container. Two kinds of elements for either make up a DP is called DPE (Data Point Element), and those that specify the format of DPs is called DPT (Data Point Type). Based on DPs, WinCC OA configures the operation panels, alarms, and stores data to the ORACLE database.

WinCC OA is made up of several managers, summed up by the Event Manager. Figure 2.1 shows the structure of managers on WinCC OA. Event Manager in the middle of the figure mediates communication between fellow managers. Database Manager reflects the operation done by WinCC OA to the database. User Interface Manager displays information sent by the Event Manager. Graphical Editor (Gedi) is the function that creates panels to display the device information and enable intuitive operation. Control Manager executes scripts on WinCC OA, using an interpreted language based on C++. It has various function libraries, and a new function can be added using C++. Application Programming Interface Manager enables to run a self-made script written in C++. Device Managers provide drivers to use devices.

Joint Control Project (JCOP) Joint Control Project (JCOP) is a framework working on WinCC OA to simplify the detector control, and DCS development [18]. The JCOP provides Finite State Machine (FSM), CAEN power supply system, DIM (Distributed Information Management system) management, trending, access control and some others. Using an interface named Device Editor Navigator (DEN), devices and FSM can be configured.

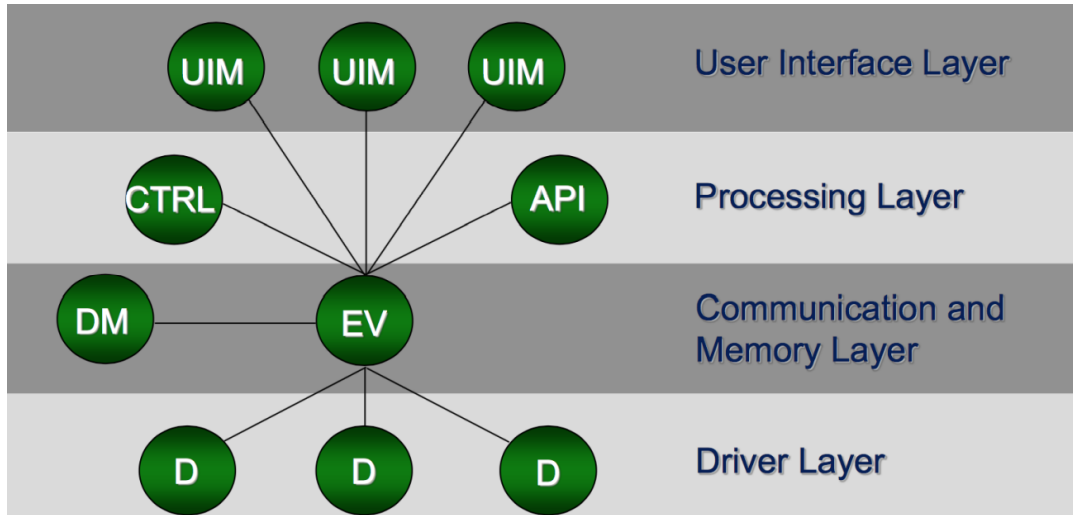


FIGURE 2.1: Structure of WinCC OA [13]

FRont-End Device (FRED) FRont-End Device (FRED) is a software to transfer data to WinCC OA directly. It connects to ALICE Low-level Front-end (ALF) running on FLP. It receives commands from WinCC OA and to ALF. Controversy, it receives DCS data from ALF and to DPs on WinCC OA. It translates hardware-level message to user-level message. It uses three types of protocols to communicate with ALF, Slow Control Adaptor (SCA), Single Word Transaction (SWT), and IC. FRED can be fully customized for detector requirements by creating a sequence file. For further customization, C++ code can be used by Message API (MAPI).

ALICE Low-level Front-end (ALF) ALICE Low-level Front-end (ALF) is a software running on FLP to communicate with FRED. It is a part of the O^2 service. ALF communicates with the CRU to collect data and send commands. Data transmission takes place in 0.5 s.

First Level Processor (FLP) First Level Processor (FLP) is a computing node for the first stage of data reduction [12]. Figure 2.2 shows the general ALICE read-out scheme. FLP is a part of O^2 , and collects the data using Common Readout Unit (CRU) from detector electronics. It divides physics data and DCS data, and sends DCS data to DCS system. It reduces the data by calibration and exclusion of physics data. It splits data by time frame and sends them to the Event Processing Node (EPN). There are 270 FLPs for the ALICE detector in total.

Common Readout Unit (CRU) Common Readout Unit (CRU) is on the FLP, and it is an interface between FEE, O^2 , and Timing Trigger System (TTS) [12]. One CRU has 24 GBT links. One FLP can host at most 2 CRUs. They are based on FPGA (Field Programmable Gate Array). CRU multiplex the data from the detector, trigger information from TTS, and control signals. Multiplexed data are sent to FLP via PCIe.

Giga-Bit Transceiver (GBT) To cope with a large amount of data in RUN-3, the upgraded data transmission links named Giga-Bit Transceiver (GBT) are applied [27]. GBT has a wide bandwidth to enable high-speed data transmission (up

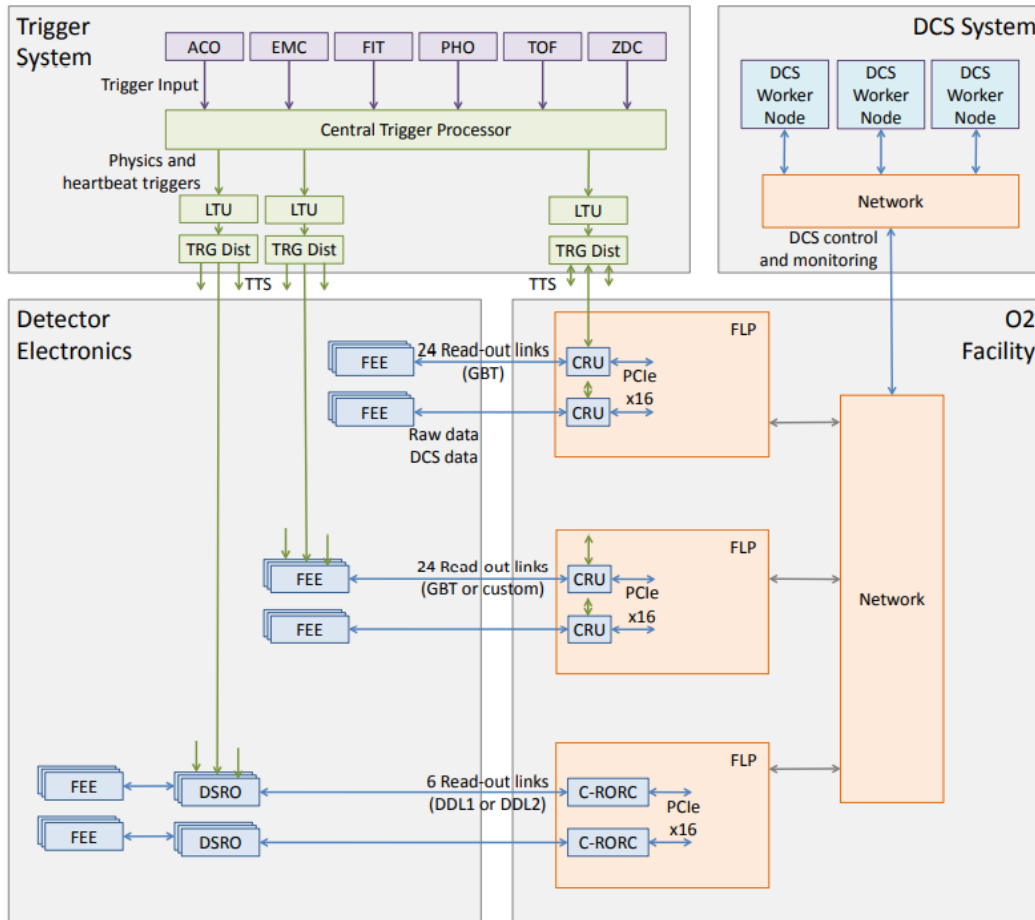


FIGURE 2.2: Architecture of O^2 , trigger and DCS [12]

to 5 GB/s). It provides simultaneous transmission of physics, trigger, and control data in the same link. GBT is a radiation tolerant system to cope with a higher level of radiation in LHC in the future. GBTx is the ASIC based on a serializer/deserializer circuit for high speed bidirectional data transmission. GBT-SCA (GBT Slow Control Adaptor) is the ASIC to provide interface for the slow controls. It has 1 I²C master, 1 SPI master, 1 JTAG master, 32 general I/O ports, 31 ADC ports, and 4 DAC ports.

Distributed Information Management (DIM) Distributed Information Management (DIM) is the CERN developed protocol that is used to communicate between WinCC OA, FRED, and ALF [17]. It runs either on Linux or Windows. DIM consists of server, client, and name server, as shown in Fig. 2.3. The server stores the information about services in name server. A client queries the name servers for information about service and obtains data from the servers. JCOP supports DIM. Its services and commands are configured on WinCC OA.

Figure 2.4 shows the DCS data flow at ALICE. ALICE DCS is based on the commercial Supervisory Control And Data Acquisition (SCADA) system called WinCC Open Architecture (WinCC OA). It is the software to manages all DCS data, sends commands to the detector, and monitor them. The DCS data management is based on the JCOP (Joint Control Project) framework. WinCC OA also provides GUI for

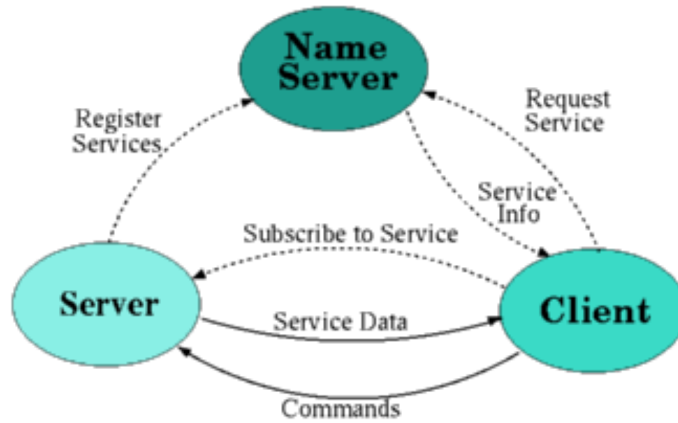


FIGURE 2.3: DIM structure [17]

operators. WinCC OA communicates with FRED (Front End Device), a software for relaying data between WinCC OA and FLP. FRED communicates with an ALICE Low-level Front-end (ALF), running on the FLP. It is the software to access CRU and transfers the DCS data to FRED, receives DCS commands from FRED, and sends them to devices. The communication protocol employed between WinCC OA, FRED, and ALF is the Distributed Information Management system (DIM) developed by CERN. CRU communicates with readout electronics and detectors via Giga-Bit Transceiver (GBT). Front-End Electronics (FEE) such as detector and readout electronics employ GBT-SCA.

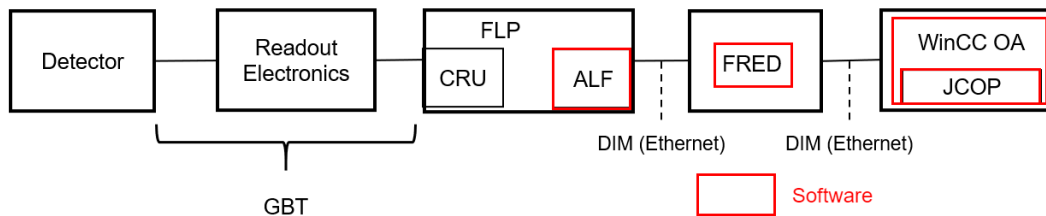


FIGURE 2.4: DCS data flow at ALICE

2.2 Architecture of the MFT DCS

2.2.1 Overview

The MFT DCS was constructed as shown in Fig. 2.5 [38, 39]. It is divided into three major parts. Multiple WinCC OA projects are used for each part, one for controlling of the power supply system, two for the detector, and one for the cooling system. The details of each element are described in the following subsections.

2.2.2 Power Supply System

CAEN products are adopted for the MFT power supply [1]. It is called CAEN EASY (Embedded Assembly System). It supplies the low voltage (LV) power to the devices

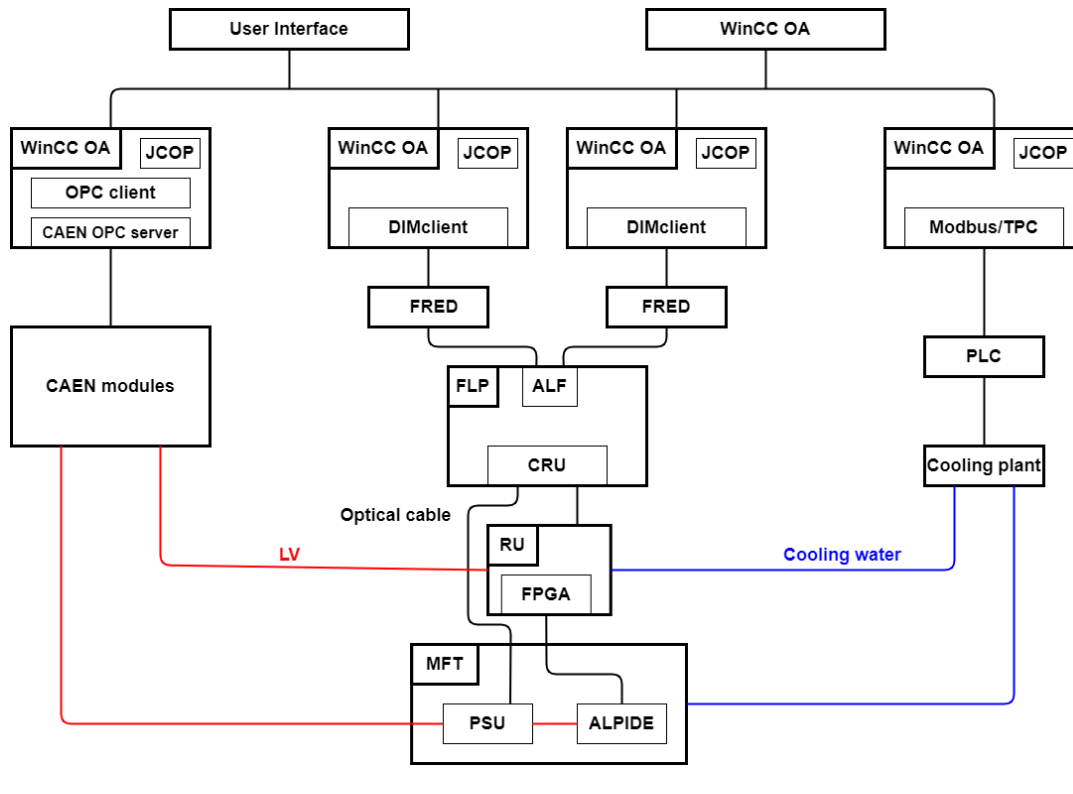


FIGURE 2.5: MFT DCS architecture

for MFT. It is controllable from WinCC OA. MFT needs LV power for PSU (Power Supply Unit), RU (Readout Unit), and PSU interface. Figure 2.6 shows the CAEN EASY architecture for MFT. Table 2.1, describes each devices. CAEN EASY is controllable from WinCC OA. JCOP provides the framework to control and monitor the CAEN by DPs. On the server, the CAEN OPC server is running to communicate with a mainframe (SY4527). OPC is the communication protocol for DCS. The mainframe (SY4527) controls the entire CAEN EASY. Two branch controllers (A1676A) are implemented on it, one is for the RUs, and the other for the PSU. Two power converters (A3486) are connected to each branch controller, one for H0 and the other for H1 separately. The power converter has two channels for the EASY3000 crate. In the two EASY3000 for RU, four A3009s are implemented. In the two EASY3000 for PSU, two A3009s and one A3006 are implemented. Those boards have channels to connect RUs and PSUs directly.

name	number	description
SY4527	1	Main frame to control entire system and communicating with the server
A1676A	2	Branch controller for easy board
A3486	4	Power converter which has 2 channels to supply 48V for crate
EASY3000	4	Crate for easy board
A3006	2	Easy board which has 6 channels $\pm(4-16)V/6A/90W$
A3009	12	Easy board which has 12 channels $\pm(2-8)V/9A/45W$

TABLE 2.1: CAEN EASY devices

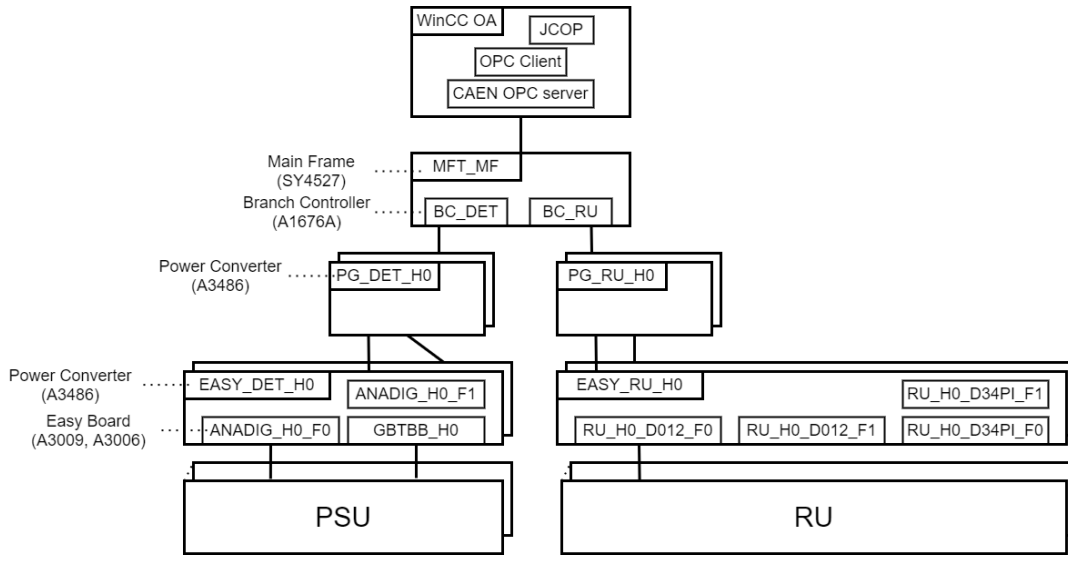


FIGURE 2.6: CAEN EASY architecture for MFT

Figure 2.7 is the LV channel number for each devices. RU has one LV input channel. Thus, it needs 80 channels in total. The A3009s provide power for them. One PSU has 13 LV input lines, 10 channels from A3009, and three channels from A3006. PSU supplies the power to the ladder. Ten channels from A3009 are to provide analog and digital voltage to the ladder. Moreover, two channels from A3006 are for back-bias voltage for the ladder, one is positive, and another is negative. The last one channels from A3006 is for GBT-SCA on PSU.

EASY boards and devices send the status data such as temperature and power status to WinCC OA. WinCC OA keeps monitoring CAEN EASY's status and sends the control signal such as voltage setting and switching on/off. The details of what elements can be monitored and manipulated can be found in the respective device manuals of CAEN [2, 3, 4, 5, 6].

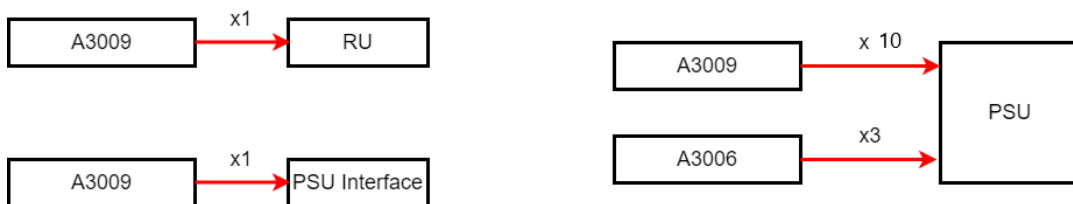


FIGURE 2.7: LV Channel number for each devices

2.2.3 Readout Unit (RU)

The RU board is the essential electronics to read data from MFT. Figure 2.8 is the picture of one RU board. MFT has 80 RUs in total. One RU needs one LV power supply channel from CAEN. They are connected to ladders equipped with ALPIDEs, and readout physics data and DCS data. RU has FPGA, GBTx, and GBT-SCA. FPGA process the readout data, and they are sent to ALICE O² by GBTx, and GBT-SCA handles the DCS data. WinCC OA gets the DCS data and controls RU by sending

commands. The hexadecimal commands are configured in the FRED, and they are sent to RU via FLP and optical link.

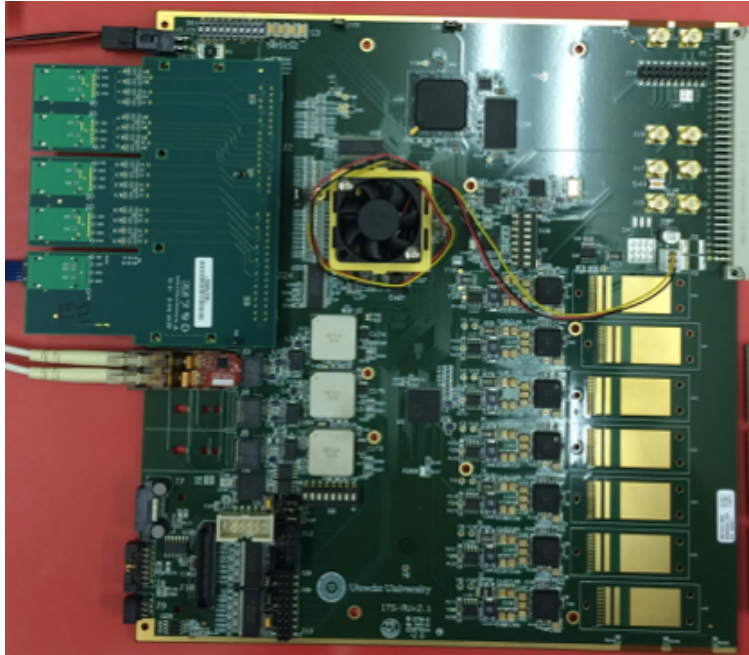


FIGURE 2.8: Readout Unit Board

The information that WinCC OA can acquire is the following.

Monitored RU status

- Temperature (GBT-SCA, FPGA, PT1000-Xilinx, PT1000-Regulators)
- Regulator voltage and current (8 power rail currents and voltages)
- Configuration Status
- Clock signals status for ALPIDEs (x5)

RU has four thermometers to detect overheating. GBT-SCA internal temperature and two PT1000 are read out from ADC ports of GBT-SCA. FPGA also has an internal thermometer. These temperature values are used to trigger interlock, which is described in Sec. 2.6. Regulators have eight power rails, and their voltages and currents can be monitored. Each of them is set to have different powers. FPGA needs configuration before starting to read data from ALPIDEs. If the setting values and readback values are consistent, the configuration status should be TRUE. In order to communicate with ALPIDEs, clock signals must be sent. Clock signals status shows whether clock signals are being sent or not.

The control signals sent from WinCC OA are as follows.

Control commands for RU

- FPGA configuration
- Setting configuration value

- Send clock signals for ALPIDEs (x5)

WinCC OA sends the configuration commands, then FRED access the database to load configuration data. Configuration data to be loaded can be changed by commands name. It is also possible to manually set the values for configuration from WinCC OA. The clock signals to ALPIDEs can be turned on and off one by one.

2.2.4 ALPIDE Chips

ALPIDEs are monitored and controlled via RU. Ladders corresponding to a single zone are connected to a single RU. They are controlled and monitored by sending commands through FLP and FRED as with the RU.

The information that WinCC OA can acquire is as follows.

Monitored ALPIDE status

- Temperature
- Active status
- Configuration status

Each chip provides a temperature value. It triggers the interlock, which is described in Sec. 2.6. When it is enabled, the active status indicates it. ALPIDEs need configuration before use. If they are configured according to the data loaded from the database, the configuration status will be TRUE.

The control signals that WinCC OA can send are following.

Control commands for ALPIDEs

- Configuration
- Setting configuration values

The configuration file for ALPIDEs is loaded from the database. It is also possible to set the values for configuration from WinCC OA.

2.2.5 Power Supply Unit

MFT has two Power Supply Units (PSU) (Fig. 2.9) for top and bottom half MFT. They are placed between disk 3 and disk 4. PSU has DC-DC converters to supply the Back-Bias, Analog, and Digital powers to a zone. One DC-DC converter is connected to 2 zones. PSU mezzanine board (Fig. 2.10) is installed one by one, and it has 5 GBT-SCAs for control. They are connected to CRU on FLP via the PSU interface. PSU interface is a board to receive and transmit data for DCS. GBT-SCA and GBTx are on it. WinCC OA gets the DCS data and controls PSU by sending commands. The commands dedicated for PSU is configured in the FRED. They are sent to PSU via FLP and optical link. Control signals are divided into PSU per disk, PSU per zone, and PSU interface.

The information of PSU per disk that WinCC OA can acquire as follows.

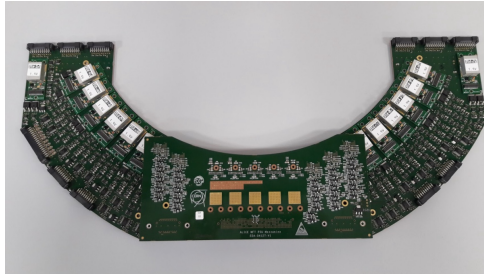


FIGURE 2.9: PSU
main



FIGURE 2.10: PSU
mezzanin board

Monitored PSU disk status

- DC-DC converter status
- Temperatures (PSU main x2, mezzanine)
- Humidity

Whether the DC-DC converters are enabled or not can be monitored, and enabling the DC-DC converter is necessary to provide the power to zones. The temperature values of the PSU main and mezzanine boards are continuously monitored. These temperature values trigger the interlock, which is described in Sec. 2.6. Furthermore, the PSU main has a humidity sensor.

The control signals of PSU per disk that WinCC OA can send are as follows.

Control commands for PSU disk

- Send configuration sequence once and starts monitoring state after
- Stop sending commands
- Enable DC-DC converter

After PSU is powered, WinCC OA needs to send the configuration sequence and start sending monitoring signals first. The stop command stops sending monitoring signals. If DC-DC converter is enabled, the corresponding zones are powered.

The information of PSU per zone that WinCC OA can acquire is as follows.

Monitored PSU zone status

- Actual values for the power supply (Analog: Current, Voltage, Threshold, Digital: Current, Voltage, Threshold, Back-Bias: Current, Voltage, Threshold)
- Latchup status

The status of power supply from the PSU is monitored by zones. The threshold value is the maximum current value to prevent the too high current due to a latchup. If the current exceeds the threshold, latch-up status becomes TRUE, and the power supply to the corresponding zones automatically stops. When a latch-up occurs, the max current is stored in the WinCC OA until the latch-up is reset.

The control signals of PSU per zone that WinCC OA can send are as follows.

Control commands for PSU zone

- Setting values for power supply (Analog: Threshold, Digital:Threshold, Back-Bias:Voltage, Threshold)
- Reset latchup

There are four kinds of setting values. They are threshold values for analog, digital, back-bias, and back-bias voltage. If a latchup occurs, a latchup reset is needed to restart the power again.

The information of PSU interface that WinCC OA can acquire is as follows.

Monitored PSU interface status

- Temperatures
- GBTx link status

PSU interface can read the temperature values from one PT1000 on board and GBT-SCA internal thermometer. These temperature values trigger the interlock. It has a primary GBTx port and an auxiliary GBTx port. WinCC OA can get the information on which GBTx is being used. The control signals of the PSU interface that WinCC OA can send are as follows.

Control commands for PSU interface

- Start configuration sequence and start monitoring state
- Reset GPT-SCA

WinCC OA begins sending the signals to the PSU interface by start command. The reset command reconfigures the GPIO ports on the GBT-SCA.

2.3 Logical Tree

A logical tree structure is defined to make it easier to handle data on WinCC OA. It is the feature provided by the JCOP framework. The tree structure based on the hardware. MFT is composed of several elements, as described in Fig. 1.13. At the bottom of the tree structure, the data corresponding to the hardware is mapped. They define aliases to the data to clarify to what channel is connected. Figure 2.11 is the logical tree for RU low voltage channels. Since RUs have one channel for one zone, the logical tree is split into 80 branches. In this case, channel000 has the alias "MFT_RU_FEE/H0/D0/F0/Z0".

To handle this channel on WinCC OA, this alias can be used instead of the hardware name. It is useful when a problem occurs with channels and the channels need to be changed because the only revision required is to reconfigure the aliases. The bottom nodes of the logical tree are assigned for all hardware channels. The following list shows all the logical trees that have been configured.

- CAEN low voltage channels for RU
- CAEN low voltage channels for PSU
- CAEN low voltage channels for PSU Interface

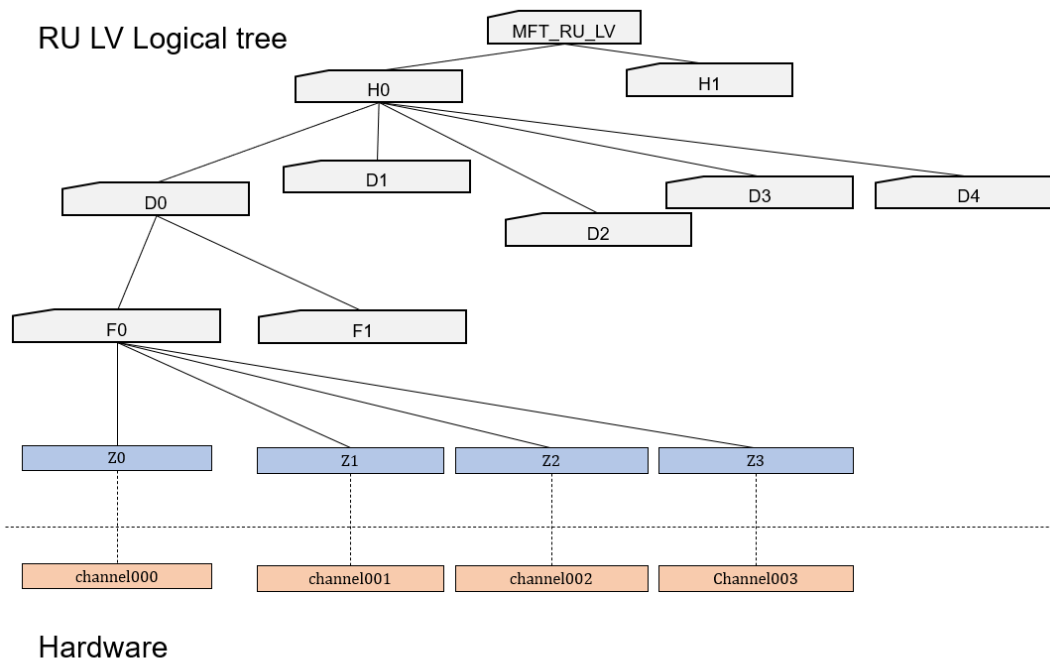


FIGURE 2.11: Logical tree for RU LV

- CAEN EASY modules
- RU FEE
- ALPIDE FEE
- PSU Disk FEE
- Low voltage channels from PSU to ladder
- PSU interface FEE

2.4 Finite State Machine

Since MFT consists of many hardware elements, the FSM is used to integrate the monitored data and simplify the control [21]. FSM is a computation model of the structure and state of the detector. The finite number of states are defined for each node. The state of a parents node is defined by its children node states. By defining the states of all the hardware elements as a tree structure, the detector state can be monitored from the top node clearly with the finite number of defined states. Also, commands can be defined for each state. Commands are sent to the lower nodes and propagated to the devices below. Therefore, a comprehensive set of operations can be defined in commands. A command is sent automatically depending on the children node's state to build an interlock system that automatically responds to abnormal conditions.

Figure 2.12 is a simple example of an FSM for the detector. The top node shows the detector's overall condition, and the state of low voltage channels and temperature sensor are associated below the top node. LV channel has ON and OFF states,

and the temperature sensor has ON and ERROR state. They depend on whether the temperature is above the threshold or not. When all the states of children are ON, the top node's state is defined to be ON. If any one of the child nodes is ERROR, the top node state must be ERROR. As Fig. 2.12, when the temperature exceeds the threshold, the temperature state goes to ERROR, and it is propagated to the upper node to turn the top node to ERROR. Then the top node automatically sends a command to switch off the low voltage channel. Hence, as shown in Fig. 2.12, the command to switch off the low voltage is sent, and its state finally goes to OFF.

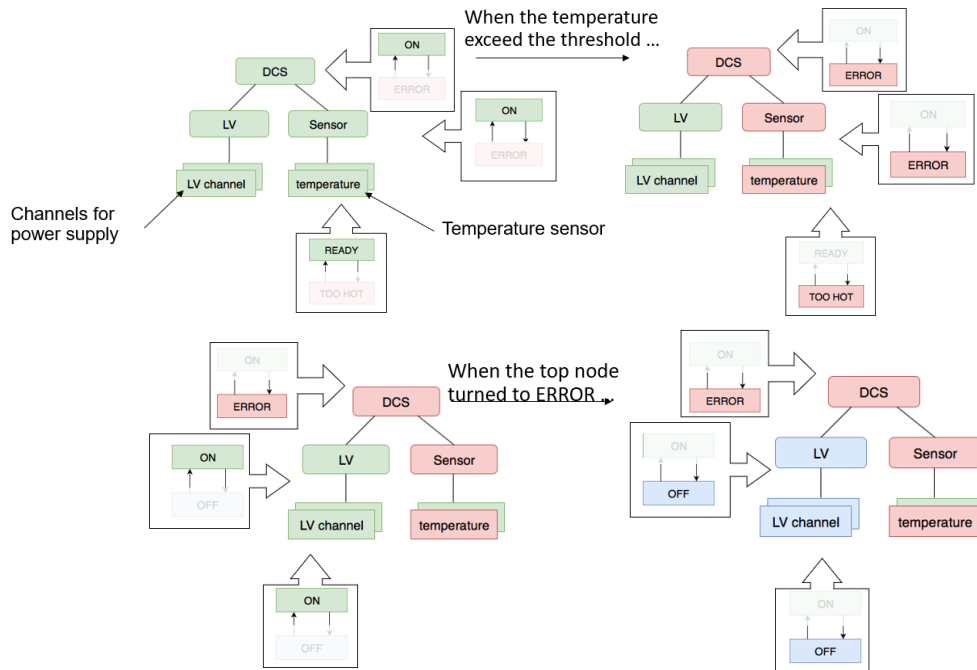


FIGURE 2.12: State transition of FSM when the temperature exceeds the threshold

Figure 2.13 is the actual FSM tree structure for MFT. The structure is divided into two below the top node, the detector part, and the infrastructure part. It is implemented in WinCC OA using the JCOP framework. Three WinCC OA projects comprise the FSM tree. There are WinCC OA projects dedicated for RU and PSU separately. In addition, a main project communicates with CAEN EASY. It also collects the data from other projects. The area indicated by the red square is configured on the WinCC OA project dedicated for PSU named `mft_psu`. The area indicated by the yellow square is configured on the WinCC OA project dedicated for RU named `mft_ru`. The other parts are configured on the main project. A control unit is a conceptual node based on the state of their children nodes, and a device unit reflects the state of the device directly. Device unit refers to the logical name described in Sec. 2.3.

Table 2.2 is the correspondence table between the states of the top node and the children nodes. The five blue states indicate no problem but not ready for the data taking, and the green state READY means it can start taking data. ERROR state is that the state needs to be recovered. Furthermore, the yellow states are the intermediate states in which the commands are in operation. Figure 2.14 is the state diagram of the MFT top node. It changes the states by executing commands such

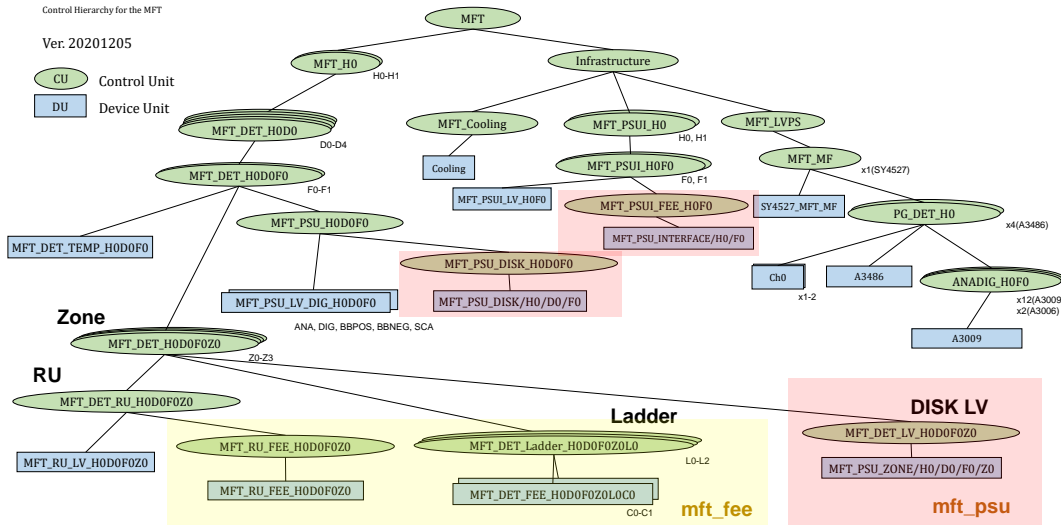


FIGURE 2.13: FSM tree structure for MFT

as "GO_READY" and "GO_OFF". To correctly start the MFT, several devices need to be enabled in the correct order. The commands defined on each state guide to the correct operation. The description by the arrow between the states shows the requirements to change the state of the node.

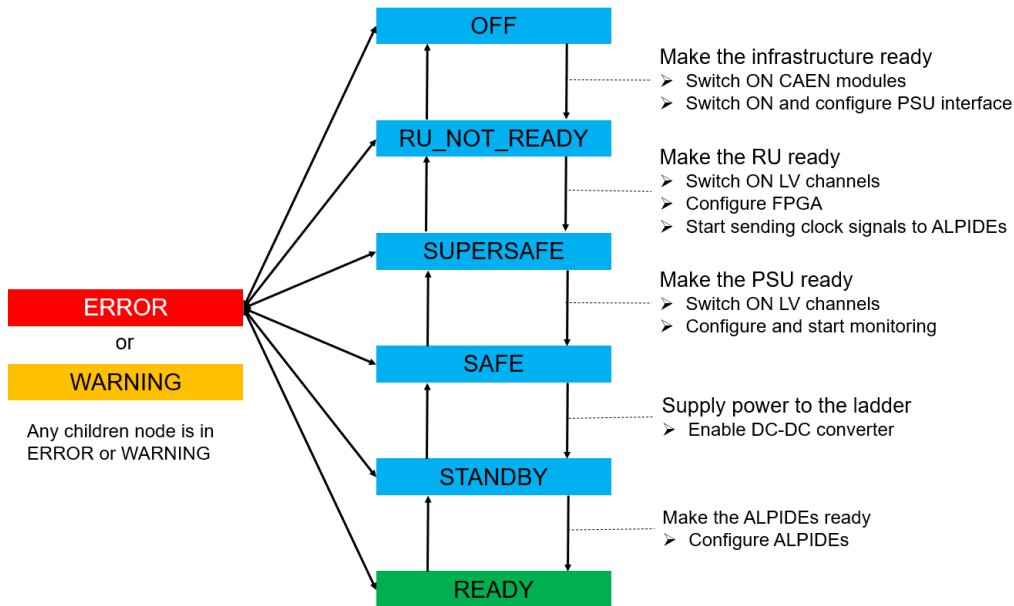


FIGURE 2.14: State diagram of the MFT top node

MFT (MFT_DCS_OT)	MFT_H0 (MFT_HALF_OT)	Infrastructure (MFT_INFRA_OT)
OFF	OFF	NOT_READY
MOVING_RU_NOT_READY	OFF	MOVING_READY
RESTORING_OFF	OFF	RESTORING_NOT_READY
RU_NOT_READY	OFF	READY
MOVING_SUPERSAFE	MOVING_SUPERSAFE	READY
RESTORING_RU_NOT_READY	RESTORING_RU_NOT_READY	READY
SUPERSAFE	SUPERSAFE	READY
MOVING_SAFE	MOVING_SAFE	READY
RESTORING_SUPERSAFE	RESTORING_SUPERSAFE	READY
SAFE	SAFE	READY
MOVING_STANDBY	MOVING_STANDBY	READY
RESTORING_SAFE	RESTORING_SAFE	READY
STANDBY	STANDBY	READY
MOVING_READY	MOVING_READY	READY
READY	READY	READY
WARNING_RU	WARNING_RU	ANY
WARNING_Ladder	WARNING_Ladder	ANY
WARNING_PSU	WARNING_PSU	ANY
WARNING_PSUI	ANY	WARNING_PSUI
ERROR_PSU	ERROR_PSU	ANY
ERROR_RU	ERROR_RU	ANY
ERROR_Ladder	ERROR_Ladder	ANY
ERROR_Latchup	ERROR_Latchup	ANY
ERROR_LVPS	ANY	ERROR_LVPS
ERROR_COOLING	ANY	ERROR_COOLING
ERROR_PSUI	ANY	ERROR_PSUI
ERROR_Unexpected	ERROR_Unexpected	ANY
UNEXPECTED STATE		

TABLE 2.2: Synchronization table of the MFT top node

2.5 Cooling system

The cooling system is needed to keep a suitable temperature. It aims to keep the temperature below 30°C and the gradient along a ladder below 5°C [36]. The cooling water system is applied for the detector and RUs, and the air cooling system is considered a backup solution. Figure 2.15 is the structure of the cooling water system for MFT. The water is brought from a common ALICE water tank to each detectors. The condition is monitored by temperature and water pressure sensors. The leakless water system is applied to the water pipe. Since the water pressure is lower than the atmosphere pressure, water will not leak even if a small hole is made in the pipe. The water pressure is set to 0.3 bar, and the temperatures are set to 18 – 20°C for detector and 18 – 23°C for RUs. All the parameters to monitor the cooling system are handled by WinCC OA.

2.6 Interlock

2.6.1 Interlock Strategy

Interlock is the system to prevent damages to machines and people. Even if the detector is damaged, it is not easy to replace the devices during the experiment. Moreover, it may damage the surrounding detectors and beam pipes. Therefore, a reliable interlock is vital for running the experiment. Two types of interlocks are

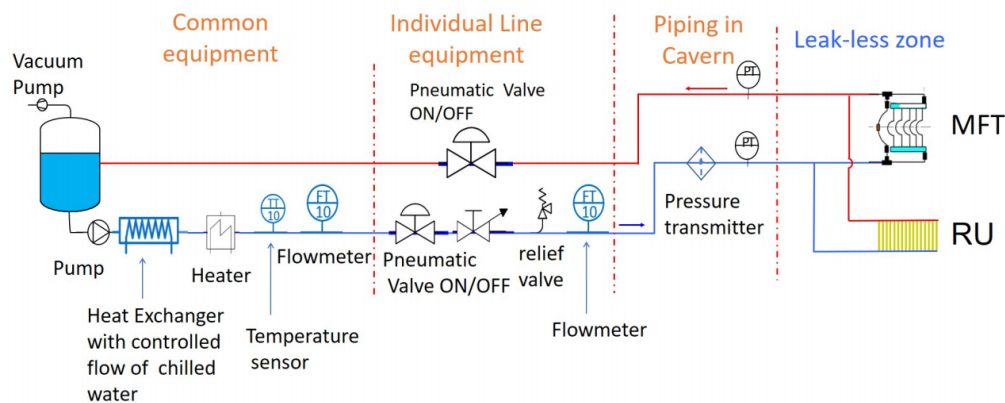


FIGURE 2.15: Structure of the water cooling system [38]

implemented for MFT to ensure safe operation [32]. If the MFT is in an abnormal state, the interlock system detects it and automatically take appropriate action.

2.6.2 Software Interlock

The FSM works as a software interlock. As shown in Fig. 2.12, state transition triggers the interlock action. Software interlocks are triggered when the devices can be damaged but do not necessarily require a quick shutdown. Temperatures and humidity are read out from MFT electronics by WinCC OA continuously. If temperature or humidity exceeds the predetermined threshold, WinCC OA turns off the corresponding LV power. If the readout digital and analog voltages are 300 mV apart, the corresponding zone is turned off. The following list summarizes the sensors that activate the software interlock to turn off the corresponding LV power.

Sensors to trigger software interlock

- half plane: Turn off LV for the corresponding half plane
 - PT100 on each plane
 - GBT-SCA internal temperature sensors on PSU
- RU: Turn off LV for the corresponding RU
 - PT1000 on board (Xilinx, regulator)
 - GBT-SCA internal temperature sensors
 - Xilinx FPGA chip internal sensors
- PSU: Turn off LV for the corresponding PSU board
 - PT100 on PSU main
 - PT100 on PSU mezzanin
 - Humidity sensor
- PSU Interface: Turn off LV for all PSU boards and then turn off LV for all PSU interface

- GBT-SCA internal temperature sensor
 - PT100 on board
- ALPIDE: Turn off LV for the corresponding zone
 - ALPIDE temperature
 - ALPIDE powers (Digital and Analog voltage)
- Cone: Turn off all the power supplies for MFT
 - Temperature sensor in MFT cone
 - Humidity sensor in MFT cone
 - Flow sensor in MFT cone

2.6.3 Hardware interlock

If a crucial problem occurs in the MFT equipment, all the MFT power needs to be stopped immediately. Detector Safety System (DSS) is the hardware interlock system used for all ALICE detectors, including MFT, to cope with those hazardous conditions. PLC (Programmable Logic Controller) on DSS is used to configure the interlock system. Figure 2.16 is the MFT DSS scheme. DSS is connected with the detector, power supply system, and cooling system. They are monitored continuously. There are two cases to trigger hardware interlock. One is a failure of the cooling system. Some sensors are implemented on the cooling system to monitor the status, and when they show abnormal values, the interlock is activated, and DSS stops all the LV channels for MFT. The other one is the communication loss with CAEN EASY. If WinCC OA lose communication with CAEN EASY, it cannot turn off the LV channels for MFT by the software interlock. To prevent this situation, if DSS can get no answer from CAEN EASY for 1 minute after sending a command, the interlock is activated, and DSS stops all the LV channels for MFT. The following list summarizes the elements that activate the hardware interlock to turn off all the power for MFT.

- Cooling water sensors [32]
 - Tank Pressure
 - Pump Pressure
 - Chilled Water Flow Temp
 - Heater Temp
 - Input Water Temp
 - Water Flow
 - Input Water Pressure
 - Output Water Pressure
 - Air Flow
 - Air Temp
- Communication loss with CAEN EASY

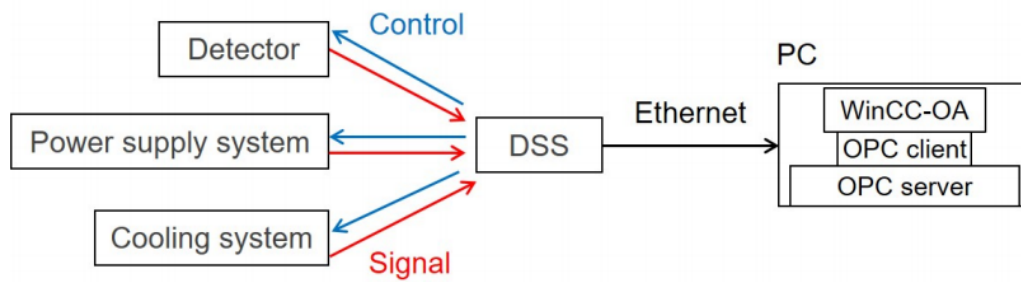


FIGURE 2.16: MFT Detector Safety System layout [38]

2.7 Operation Panel

GUI panels are developed on WinCC OA. They are connected to DPs via a logical tree. They show the status of devices and send the control signal. They are developed at the level corresponding to the FSM tree. The operation items available by FSM are summarised in a panel. There are panels for the standard users and the expert users separately. Some controls are prohibited in the standard user panel compared to the expert panel. Figure 2.17 shows the standard user panel for the top MFT node, and Fig. 2.18 shows the expert user panel for the top MFT node.



FIGURE 2.17: The standard user panel for top MFT node



FIGURE 2.18: The expert panel for top MFT node

Chapter 3

Operation Test

3.1 DCS Test Bench at Hiroshima

3.1.1 Overview

The newly developed functions of DCS are tested before being implemented to the actual devices. A DCS test bench has been constructed at Hiroshima University [30]. It is composed of the equipment and software used for MFT. Figure 3.1 is the structure of the DCS test bench at Hiroshima. It is a set of computers needed for DCS and MFT devices to be controlled. The number of channels is less than the actual MFT, but every control for MFT can be tested using the test bench. The top node in Fig. 3.1 is the WinCC OA. There are one RU, one ladder, one PSU, and one PSU interface in Hiroshima. They are connected to CRU on FLP via an optical link. Through this structure, the WinCC OA sends commands and receives the DCS data from the devices. The main functions of DCS, such as panels and FSMs, are configured on the WinCC OA. The CAEN simulator, as a software on WinCC OA, is used instead of the actual power supply system. The WinCC OA project at CERN is updated if the normal operation is ensured with newly implemented functions through tests with the test bench.

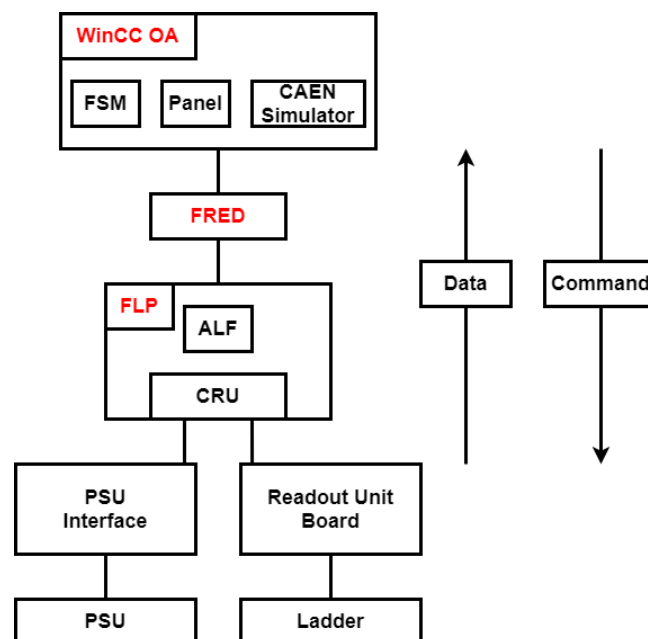


FIGURE 3.1: The structure of the DCS test bench at Hiroshima

3.1.2 RU test

The FSM and panel for RU are tested with the test bench. Figure 3.2 is the picture of RU and ladder. They are the same as the actual devices for MFT. The panel and FSM for the RU are confirmed with the test bench. Figure 3.3 is the RU operation panel for the experts. Using the panels, MFT user monitors the low voltage channel's status from CAEN EASY, FPGA configuration, temperatures on board, regulator voltage and current, and the communication with ALPIDEs. In the test bench, they were monitored correctly, and the trend was displayed on a graph. As for the configuration and ALPIDEs controls, it was confirmed that they could be controlled by pressing a button on the panel. When the configure command is sent to FRED, configuration values are loaded from a database at CERN. Several types of configuration value sets are stored at the database. Configure command selects one of them and load the values. FRED compares the configuration values loaded from the database and the read back values from the RU. If they are consistent, FRED send the signal to indicate that the configuration is complete.

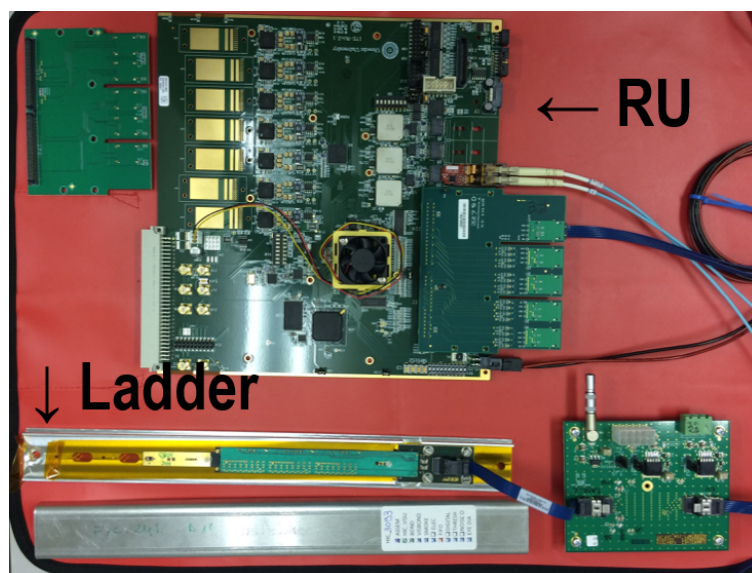


FIGURE 3.2: RU and Ladder in the test bench

Figure 3.4 is the FSM tree for RU. The RU node has the children nodes that represent the state of the RU FEE and the state of the LV channel. The RU FEE shows the status of electronics on RU board, such as FPGA. The LV channels is the power line that is supplied the power to RU. The RU has six stable states. They are OFF, STANDBY, CONFIGURED, READY, WARNING, and ERROR. What each state represents for the devices is noted next to the table in Fig. 3.4. Each node has defined actions to change its state. The RU FSM was tested if the FSM state changes correctly by executing actions and changing the temperature. When GO_READY command was executed, the channels were turned on, and the FPGA on RU was configured. Then, the state goes to READY as Fig. 3.5. The temperatures are displayed in the panel on the right side, and the RU FSM states are displayed on the left side. When the temperature rises and the GBT-SCA internal thermometer or the PT1000 on boards exceeds 50 °C, the RU FEE state goes to ERROR. And then, the ERROR state of RU FEE triggered the automatic power off. Figure 3.6 is the moment that the command to turn off the LV channel has just been sent. After that, when the RU cooled down

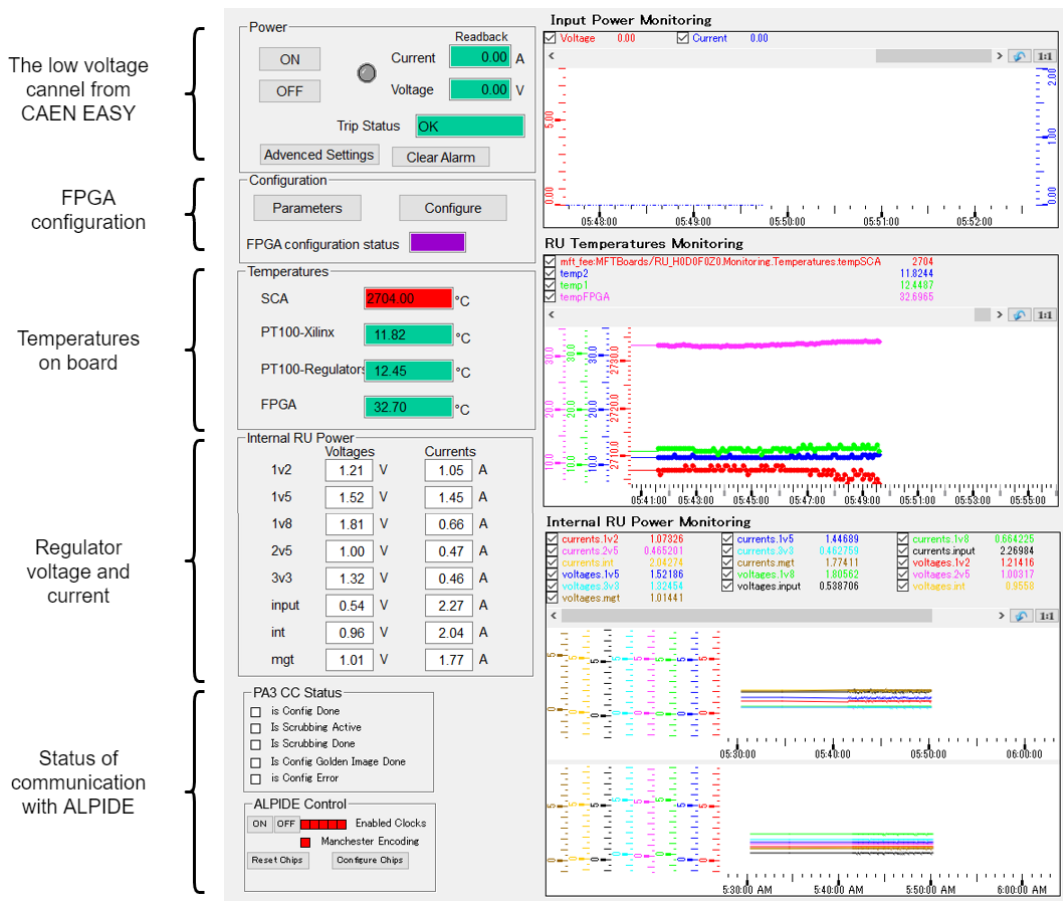


FIGURE 3.3: RU panel

and the temperature was between 30 °C and 50 °C, the state became WARNING, as Fig. 3.7. It confirmed that the state transition and interlocks were working correctly with the FSM.

3.2 Surface Commissioning at CERN

3.2.1 Overview

For one year from October 2019, the whole MFT was tested on the ground at CERN. It is a phase called the surface commissioning. During the surface commissioning, the MFT was assembled, and the operation tests had been conducted. RU, CAEN EASY, and computing systems including FLP and FRED are also connected as the actual run. Figure 3.8 is the half MFT and MFT collaboration member at commissioning room. Figure 3.9 is the half MFT just after it is assembled, and Fig. 3.10 is the RU and CAEN modules in the racks at the commissioning room. A part of the DCS was installed in the system to test monitoring and controlling the detector. The control system for CAEN EASY and RUs was commissioned.

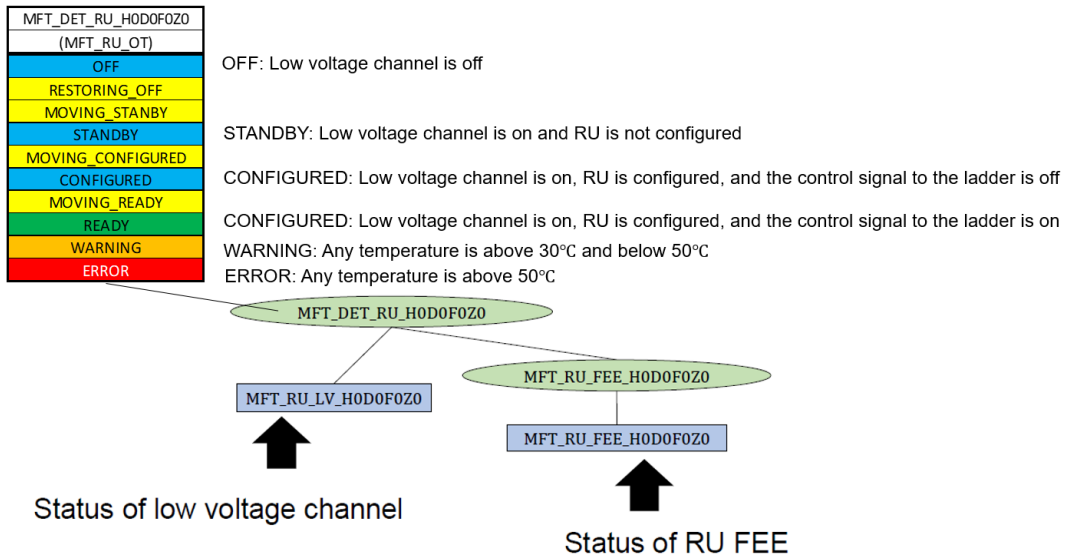
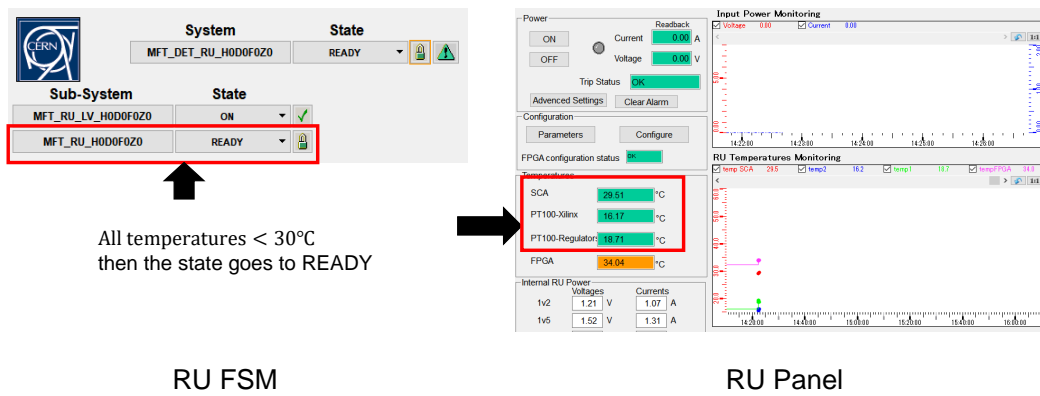
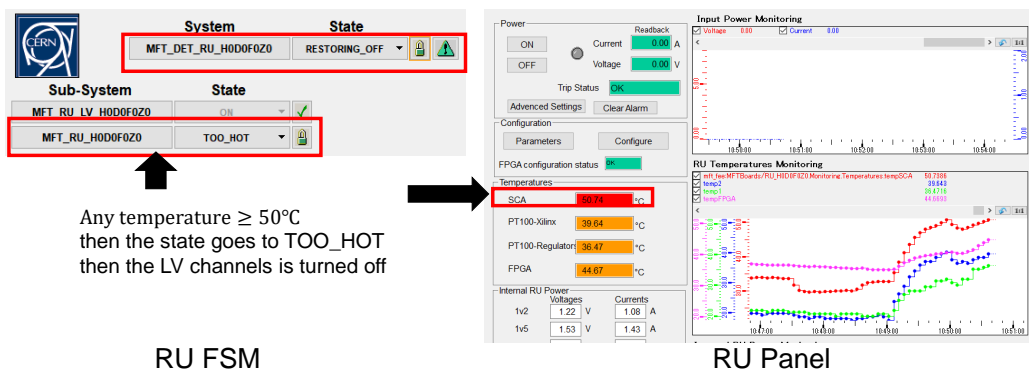


FIGURE 3.4: FSM tree for RU



All temperatures < 30°C then the state goes to READY

FIGURE 3.5: RU FSM test 1:Ready state



Any temperature ≥ 50°C then the state goes to TOO_HOT then the LV channels is turned off

FIGURE 3.6: RU FSM test 2:RU error state

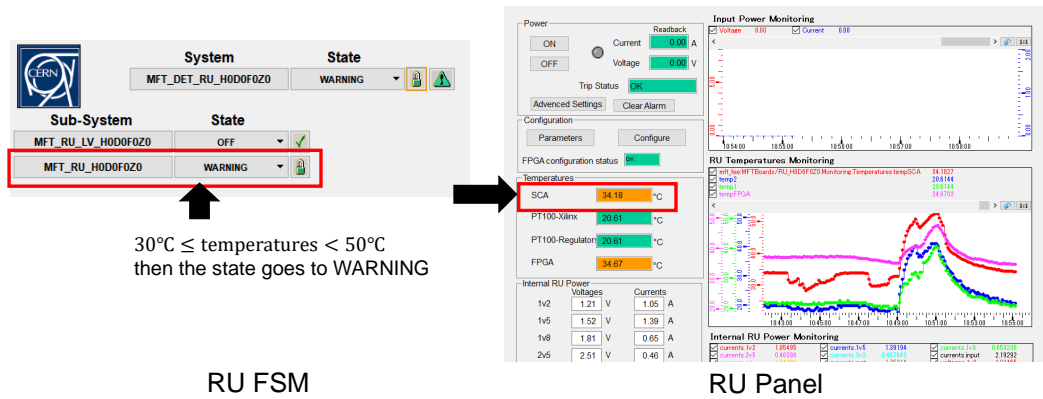


FIGURE 3.7: RU FSM test 3:RU warning state

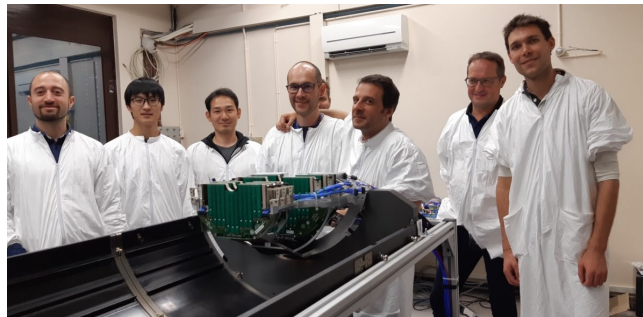


FIGURE 3.8: The half MFT and MFT collaboration member at commissioning room

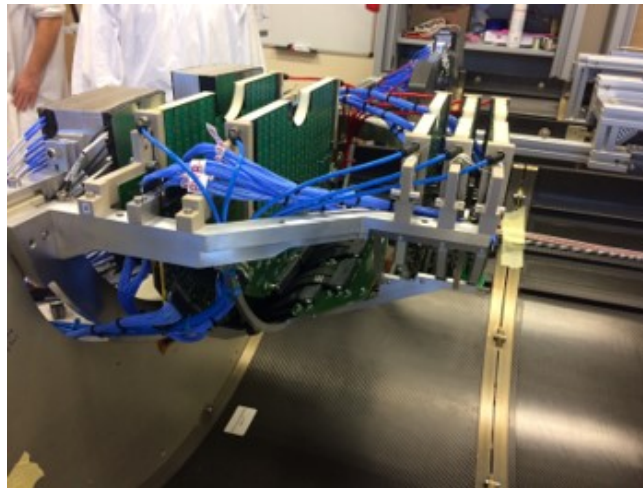


FIGURE 3.9: MFT at commissioning room

3.2.2 CAEN EASY test

CAEN EASY, which is the power supply system for MFT, was tested in the surface commissioning. It supplies low voltage power to the RUs and PSUs. First, the control of each channel was tested. Figure 3.11 is the panel to control the channel on the

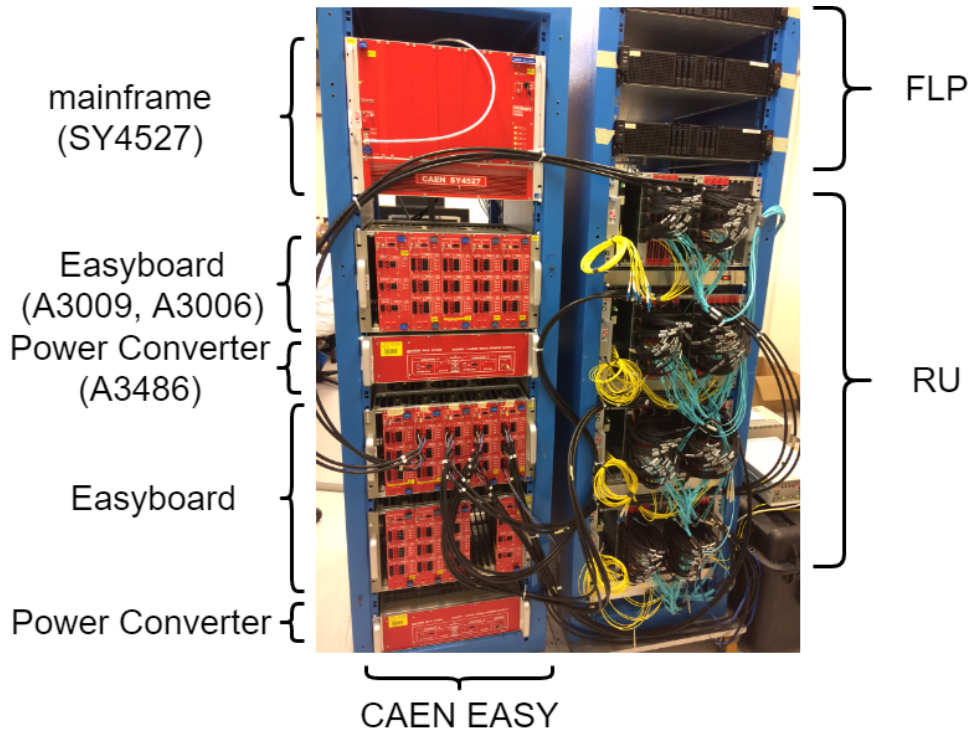


FIGURE 3.10: RU and CAEN at commissioning room

power generator. It kept monitoring the voltage, current, and their trends, the power state, temperature. The ON/OFF button worked correctly, and detailed settings can be defined from an additional panel popping up by clicking the "Advanced Settings" button.

As described in Fig. 3.10, CAEN EASY is composed of the mainframe (SY4527) with the branch controller (A1676A), Easyboards (A3009, A3006), and power converters (A3486). Detail of CAEN EASY is described in Section 2.3. The states of these devices are monitored by FSM. Figure 3.12 is the FSM states for the CAEN EASY at the commissioning room. The status of LVPS (Low Voltage Power Supply) and its child nodes are displayed. Available commands can be selected from the pull-down menu. When the abnormal state is detected, these nodes move from READY to ERROR and propagate their states to the higher-level nodes. It was confirmed that the FSM state represents the status of devices correctly. Available commands are defined for each state. If it is the NOT_READY state as Fig. 3.12, available commands are CLEAR_ALARM and GO_READY. CLEAR_ALARM clears the information of the alarm when an error occurred, and restore the normal state from alarm state. GO_READY turns on the channels on power converters to enable all Easyboards. It was confirmed that CAEN EASY works correctly by these commands.

3.3 Installation and Commissioning at P2

The MFT was installed in the ALICE detector in a cavern in November 2020 (Fig. 3.13). Currently, the final commissioning for the LHC RUN-3 is being conducted. The DCS is deployed to the computing system at P2, where is the experimental area of ALICE. It is in a special network that only the access by the granted users is allowed from outside of P2. It has three worker nodes for DCS. WinCC OA projects for the CAEN,

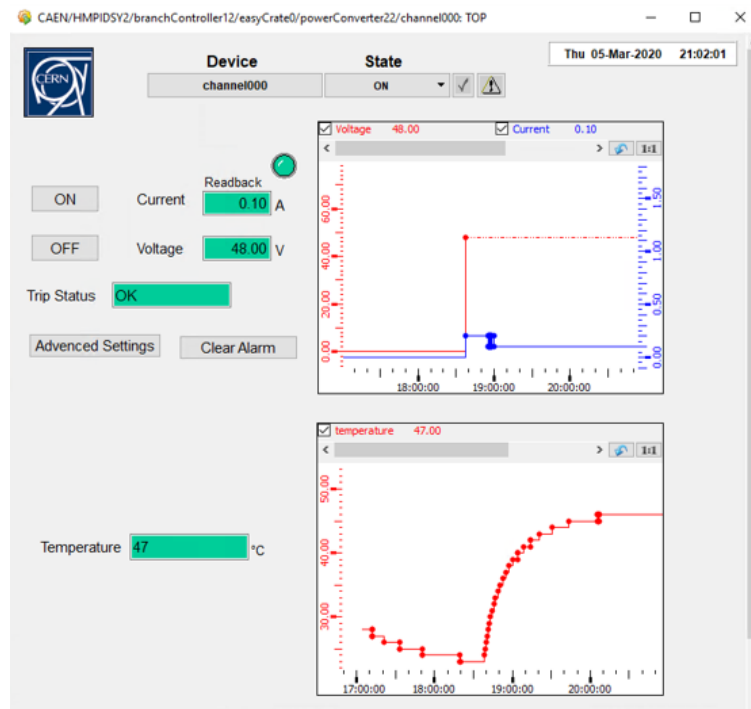


FIGURE 3.11: Panel for channel on power converter

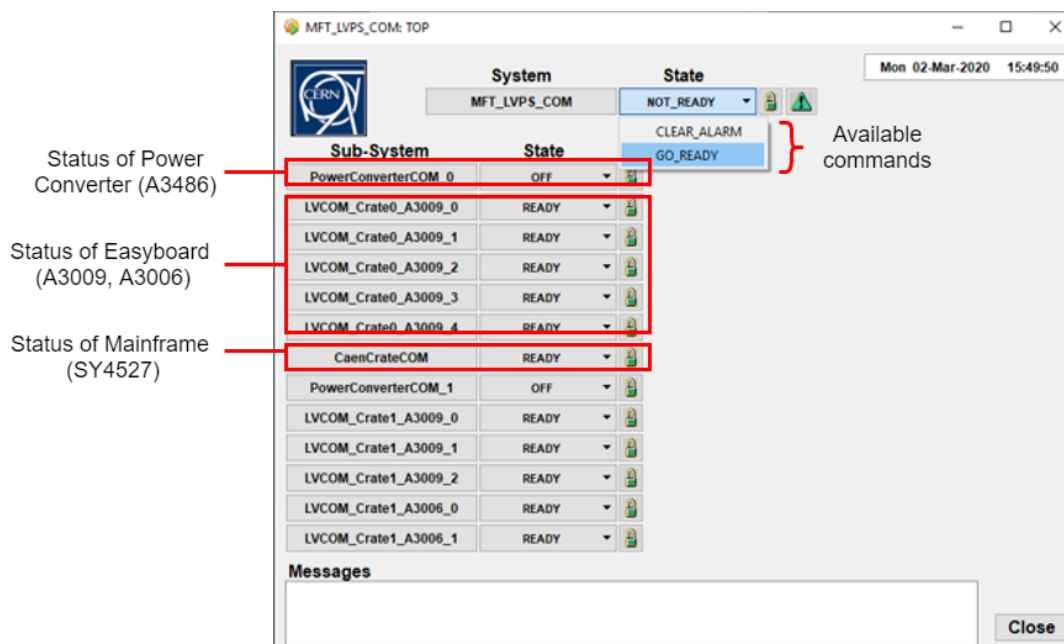


FIGURE 3.12: FSM states for the CAEN EASY

RU, and PSU are deployed to the separate worker nodes. The FRED server is also in a DCS network. In addition to that, the operator node is prepared for operators. GUIs on the WinCC OA can be used from the operator node.

The functions of the panel, FSM, and the operation of the devices were tested with the actual MFT.

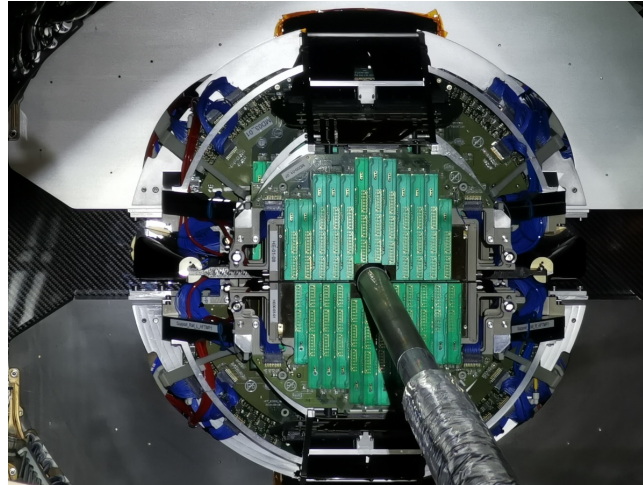


FIGURE 3.13: MFT installed in a cavern

3.3.1 CAEN EASY test

CAEN EASY was installed in the process management layer, which is located at the level between the ground and the detector levels in the cavern. All the channels were connected to the RU and PSU properly, and they were tested to see if they work correctly. Some panels to control MFT can be used on the operator node. Figure 3.14 is the CAEN channel panel for RU H0D0. The panel monitored the status, turn channels ON/OFF, and set values, just as it had done in the surface commissioning.

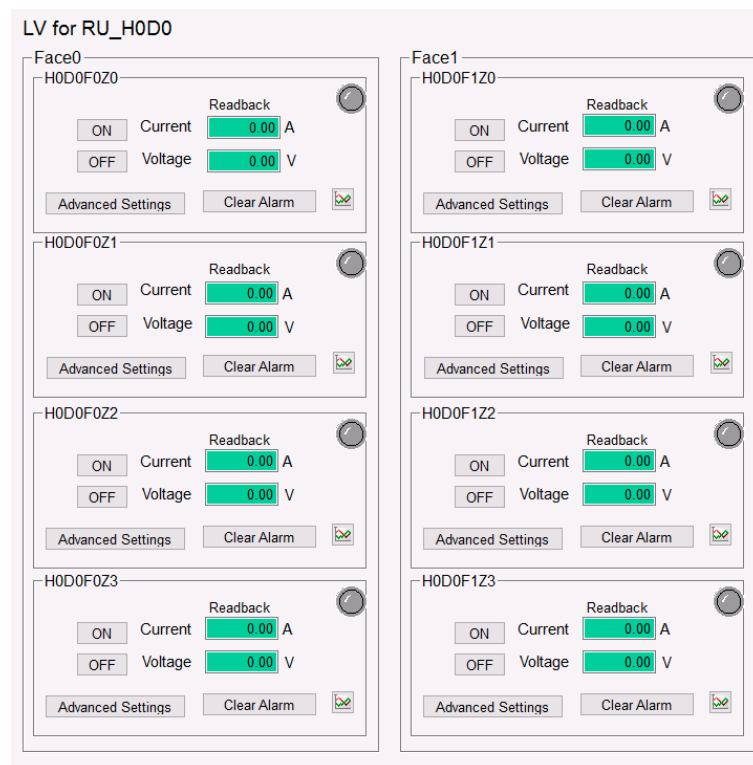


FIGURE 3.14: CAEN channel panel for RU H0D0

3.3.2 PSU test

The PSU operation was tested at P2. Figure 3.15 is the operation panel for PSU disk H0D0F0. By pressing the start button, PSU information described in Sec.2.2.2 could be monitored. Sending the control commands is also tested. The latchup reset and enabling DC-DC converter were confirmed to work correctly.



FIGURE 3.15: PSU panel tested at P2

Chapter 4

Summary

4.1 Conclusion

In this study, the detector control system for the muon forward tracker has been developed. The new system to handle DCS data has been constructed to match the new computing system, O^2 . The DCS dedicated to the MFT is mainly developed on WinCC OA. From the WinCC OA, it is now possible to monitor all information and send control signals. GUIs are created for the standard users and experts. Besides, the finite state machine with a hierarchical logical structure is created based on the hardware. It enables comprehensive control and easy monitoring of the detector. It also acts as the interlock to ensure a safe operation. These DCS functions had been tested and confirmed with the actual devices. The first test was done using the DCS test bench at Hiroshima, and it was implemented with the MFT for the first time in the surface commissioning. The operation of some devices is confirmed there. Finally, it is implemented in the ALICE cavern, and the final tests before the LHC RUN-3 has been conducted.

4.2 Outlook

After all DCS functions are assured, a stand alone commissioning of MFT will be conducted in the first half of 2021. Then, in the global commissioning, the final test for the operation will be conducted with other ALICE detectors. LHC RUN-3 will start from 2022. In the meantime, DCS will be used to operate the MFT and take data. While it is taking data, the status of MFT is constantly monitored, and if an error is detected, it will be fixed every time.

Appendix A

Logical Tree

A logical tree is an alias for device status data on WinCC OA. It is described on Sec. 2.3. The logical tree for each devices are as follows.

A.1 RU FEE

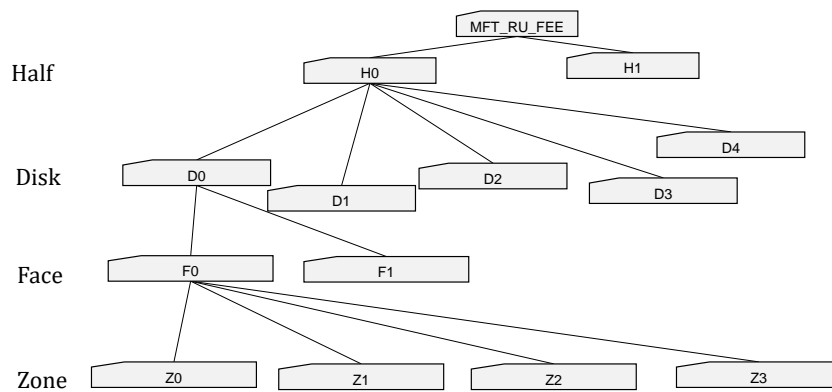


FIGURE A.1: Logical tree of RU FEE

A.2 DISK FEE

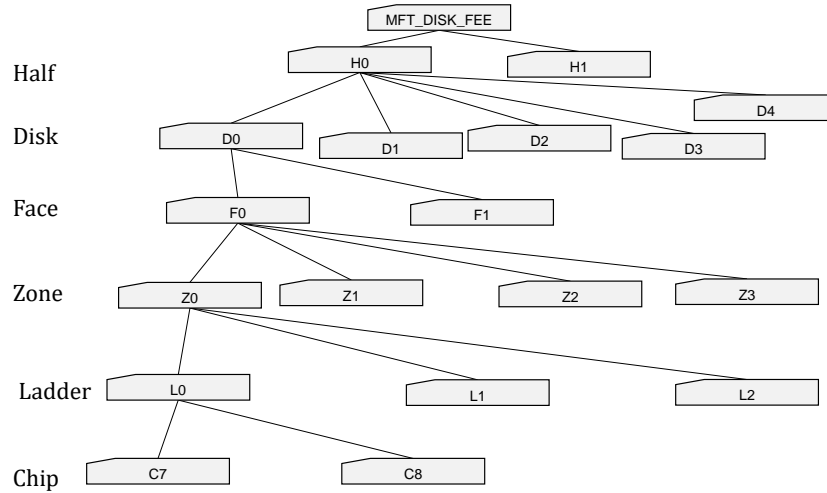


FIGURE A.2: Logical tree of DISK FEE

A.3 PSU ZONE

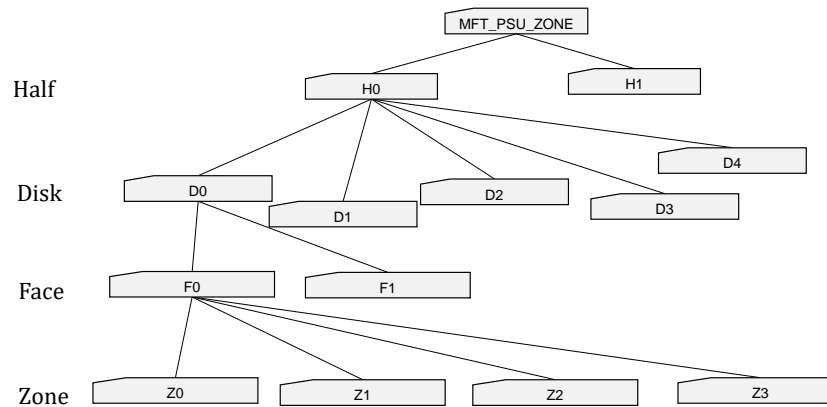


FIGURE A.3: Logical tree of PSU ZONE

A.4 PSU DISK

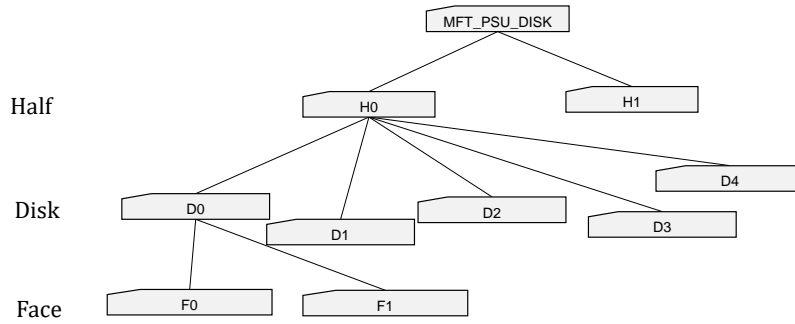


FIGURE A.4: Logical tree of PSU DISK

A.5 PSU INTERFACE

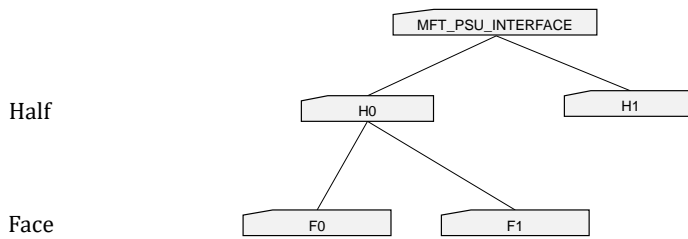


FIGURE A.5: Logical tree of PSU INTERFACE

A.6 RU LV

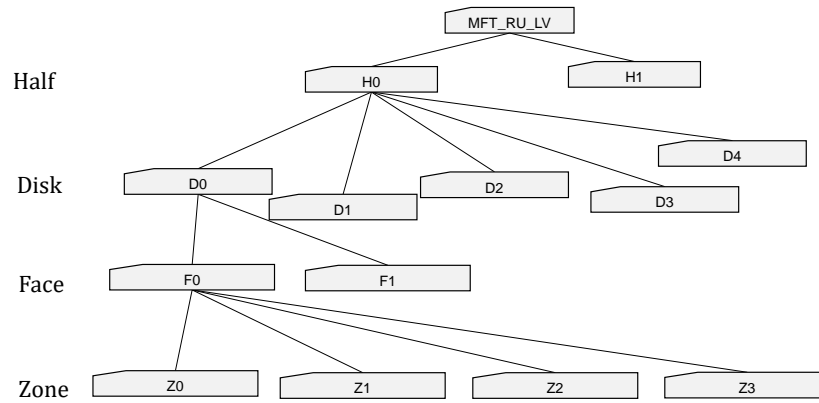


FIGURE A.6: Logical tree of RU LV

A.7 PSU LV

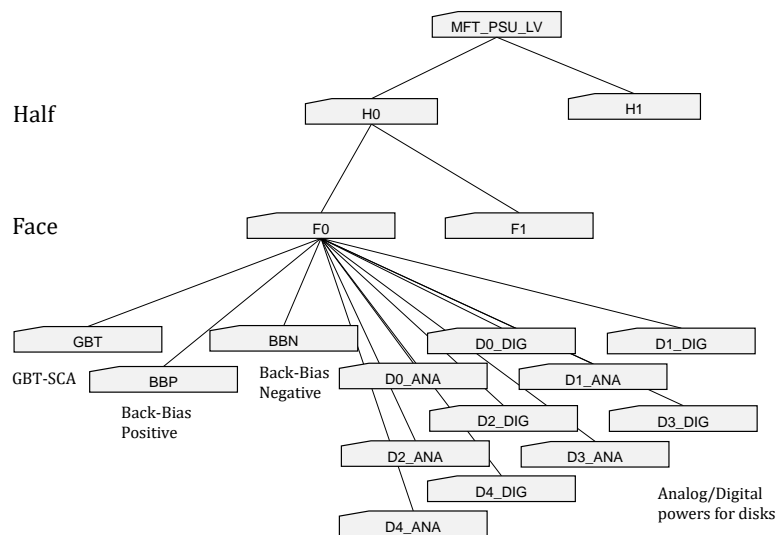


FIGURE A.7: Logical tree of PSU LV

A.8 PSU INTERFACE LV

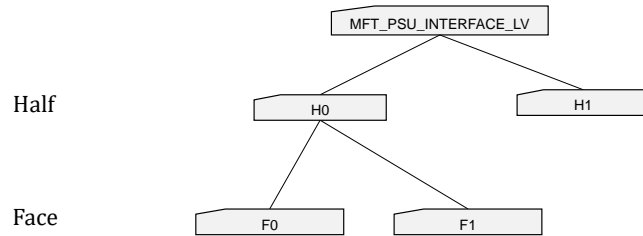


FIGURE A.8: Logical tree of PSU INTERFACE LV

A.9 CAEN EASY

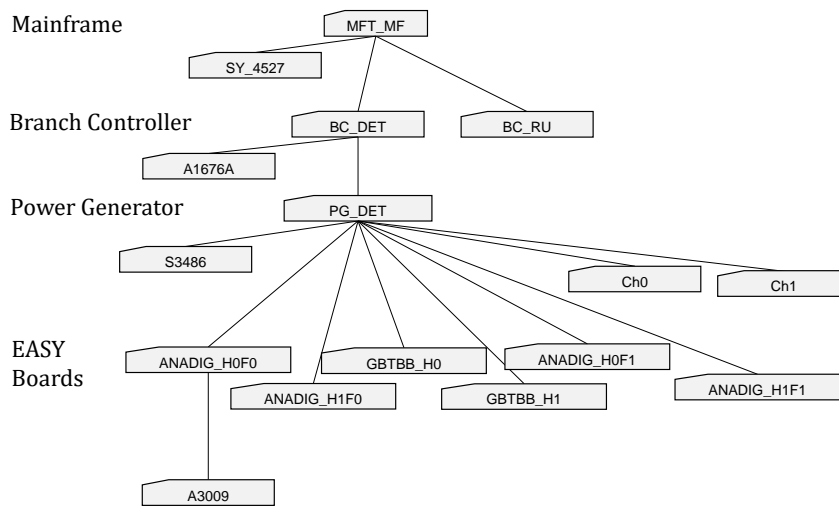


FIGURE A.9: Logical tree of CAEN EASY

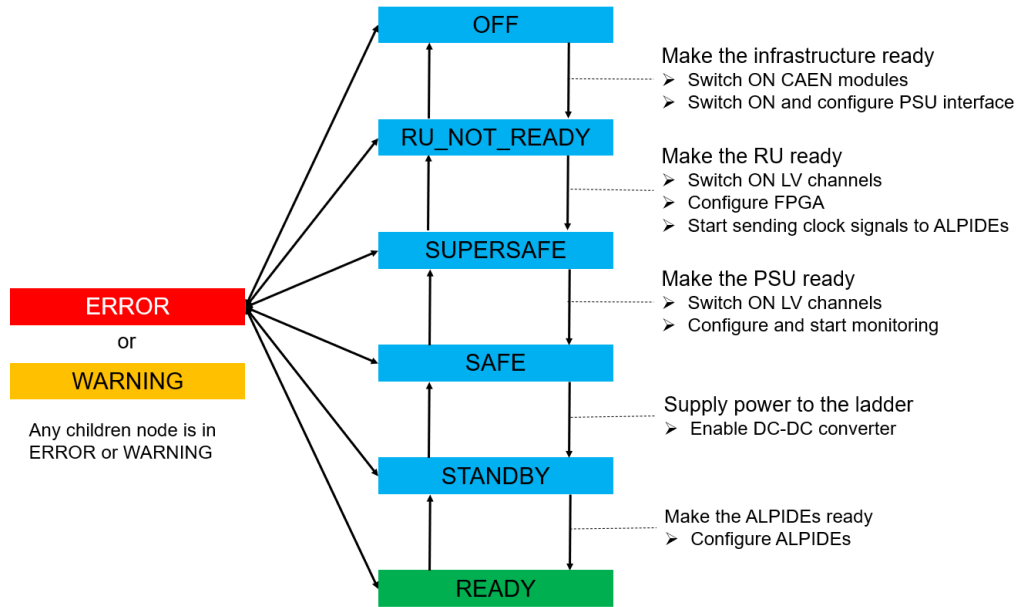


FIGURE B.3: The state diagram for MFT top node

MFT (MFT_DCS_OT)	MFT_H0 (MFT_HALF_OT)	Infrastructure (MFT_INFRA_OT)
OFF	OFF	NOT_READY
MOVING_RU_NOT_READY	OFF	MOVING_READY
RESTORING_OFF	OFF	RESTORING_NOT_READY
RU_NOT_READY	OFF	READY
MOVING_SUPERSAFE	MOVING_SUPERSAFE	READY
RESTORING_RU_NOT_READY	RESTORING_RU_NOT_READY	READY
SUPERSAFE	SUPERSAFE	READY
MOVING_SAFE	MOVING_SAFE	READY
RESTORING_SUPERSAFE	RESTORING_SUPERSAFE	READY
SAFE	SAFE	READY
MOVING_STANDBY	MOVING_STANDBY	READY
RESTORING_SAFE	RESTORING_SAFE	READY
STANDBY	STANDBY	READY
MOVING_READY	MOVING_READY	READY
READY	READY	READY
WARNING_RU	WARNING_RU	ANY
WARNING_Ladder	WARNING_Ladder	ANY
WARNING_PSU	WARNING_PSU	ANY
WARNING_PSUI	ANY	WARNING_PSUI
ERROR_PSU	ERROR_PSU	ANY
ERROR_RU	ERROR_RU	ANY
ERROR_Ladder	ERROR_Ladder	ANY
ERROR_Latchup	ERROR_Latchup	ANY
ERROR_LVPS	ANY	ERROR_LVPS
ERROR_COOLING	ANY	ERROR_COOLING
ERROR_PSUI	ANY	ERROR_PSUI
ERROR_Unexpected	ERROR_Unexpected	ANY
UNEXPECTED STATE		

FIGURE B.4: The synchronization table for MFT top node

B.3 Infrastructure node

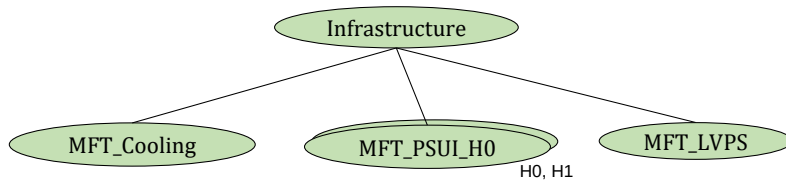


FIGURE B.5: The sub-tree structure of infrastructure

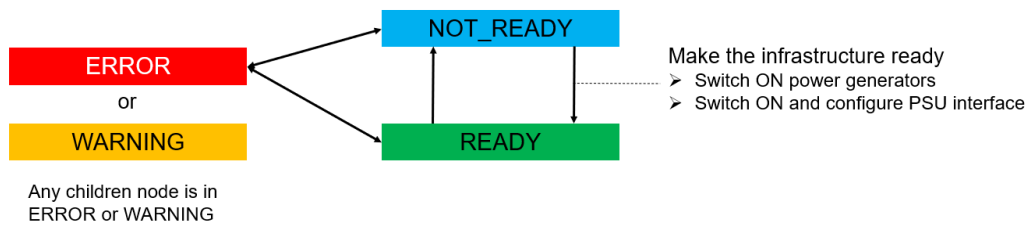


FIGURE B.6: The state diagram for infrastructure

Infrastructure (MFT_INFRA_OT)	MFT_LVPS (MFT_LVPS_OT)	MFT_Cooling (MFT_COOLING_OT)	MFT_PSUI_H0 (MFT_PSUIINTERFACE_HALF_OT)
NOT_READY	NOT_READY	ANY	ANY
	ANY	NOT_READY	ANY
	ANY	ANY	OFF
MOVING_READY	MOVING_READY	READY	MOVING_ON
RESTORING_NOT_READY	RESTORING_OFF	READY	RESTORING_OFF
READY	ON	READY	ON
WARNING_PSUI	ANY	ANY	WARNING
ERROR_LVPS	ERROR	ANY	ANY
ERROR_COOLING	ANY	ERROR	ANY
ERROR_PSUI	ANY	ANY	ERROR

FIGURE B.7: The synchronization table for infrastructure

B.4 LVPS node

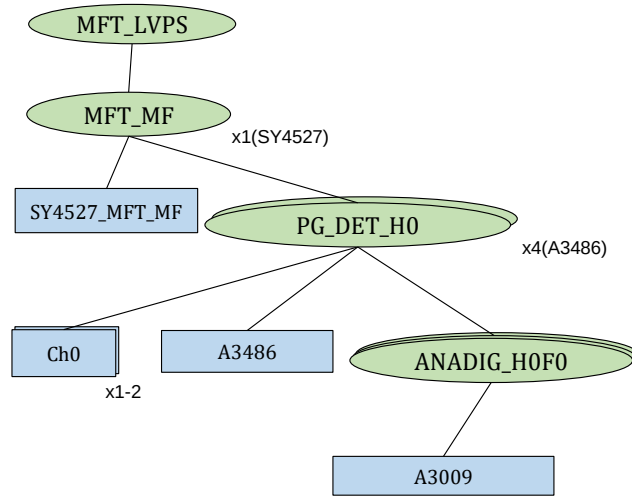


FIGURE B.8: The sub-tree structure of LVPS

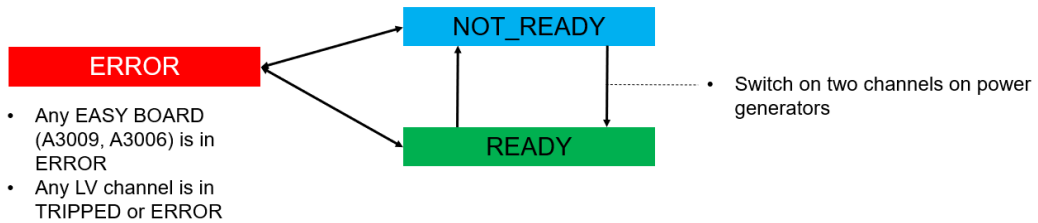


FIGURE B.9: The state diagram for LVPS

MFT_LVPS	MFT_MF
(MFT_LVPS_OT)	(MFT_CAENCRATE_OT)
NOT_READY	NOT_READY
MOVING_READY	MOVING_READY
RESTORING_OFF	RESTORING_OFF
READY	READY
ERROR	ERROR

FIGURE B.10: The synchronization table for LVPS

MFT_MF (MFT_CAENCRATE_OT)	PG_DET (MFT_48VPS_OT)	SY4527_MFT_MF (FwCaenCrateSY1527)
NOT_READY	OFF	READY
MOVING_READY	MOVING_ON	READY
RESTORING_OFF	RESTORING_OFF	READY
READY	ON	READY
ERROR	ERROR	ANY
	ANY	ERROR

FIGURE B.11: The synchronization table for mainframe

PG_DET (MFT_48VPS_OT)	A3486_PG_DET (FwCaenBoardEasy)	Ch0 (FwCaenChannel)	ANADIG_H0F0 (MFT_EASYBOARD_OT)
OFF	ANY	OFF	ANY
MOVING_ON	ANY	OFF→ON	ANY
RESTORING_OFF	ANY	ON→OFF	ANY
ON	READY	ON	READY
ERROR	ERROR	ANY	ANY
	TOO_HOT	ANY	ANY
	ANY	TRIPPED	ANY
	ANY	ERROR	ANY
	ANY	ANY	ERROR

FIGURE B.12: The synchronization table for generator

B.5 PSU interface node

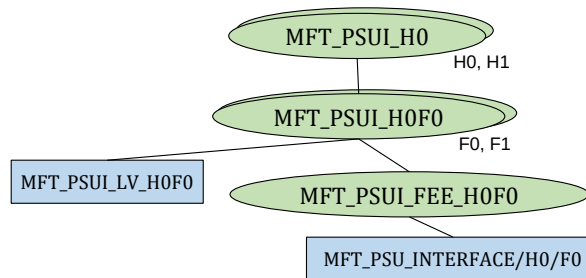


FIGURE B.13: The sub-tree structure of PSU interface

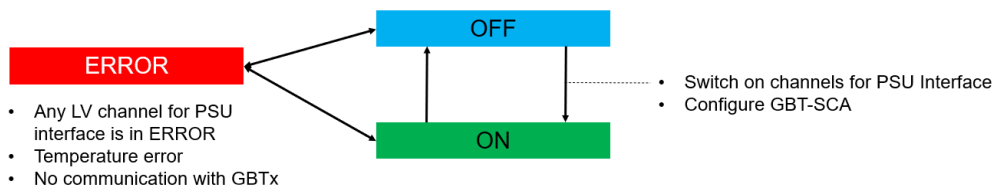


FIGURE B.14: The state diagram for PSU interface

MFT_PSUI_H0 (MFT_PSUIINTERFACE_HALF_OT)	MFT_PSUI_H0F0 (MFT_PSUIINTERFACE_FACE_OT)
OFF	OFF
MOVING_ON	MOVING_ON
RESTORING_OFF	RESTORING_OFF
ON	ON
WARNING	WARNING
ERROR	ERROR

FIGURE B.15: The synchronization table for PSU interface half

MFT_PSUI_H0F0 (MFT_PSUIINTERFACE_FACE_OT)	MFT_PSUI_LV_H0F0 (FwCaenChannel)	MFT_PSUI_FEE_H0D0F0 (MFT_PSU_INTERFACE_OT)
OFF	OFF	OFF
MOVING_ON	OFF→ON	MOVING_ON
RESTORING_OFF	ON→OFF	RESTORING_OFF
ON	ON	ON
WARNING	ANY	WARNING
ERROR	ERROR	ANY
	ANY	ERROR

FIGURE B.16: the synchronization table for psu interface face

MFT_PSUI_FEE_H0D0F0 (MFT_PSU_INTERFACE_OT)	MFT_PSU_INTERFACE/H0/F0 (MFT_PSUInterface)
OFF	OFF
MOVING_ON	OFF→ON
RESTORING_OFF	ON→OFF
ON	ON
WARNING	WARNING
ERROR	ERROR

FIGURE B.17: the synchronization table for psu interFEE FEE

B.6 Half node

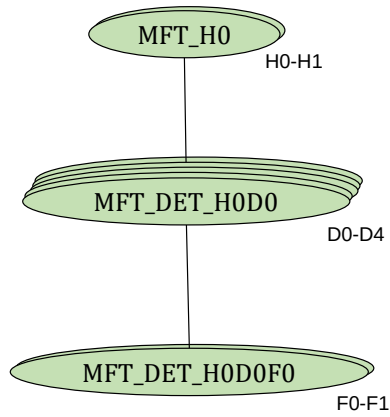


FIGURE B.18: The sub-tree structure of half

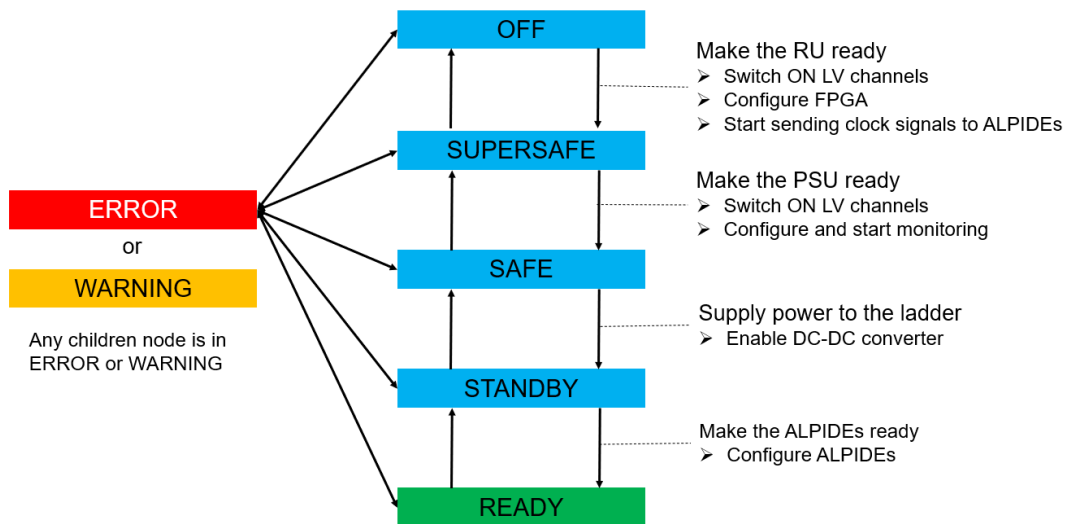


FIGURE B.19: The state diagram for half

MFT_H0 (MFT_HALF_OT)	MFT_DET_H0D0 (MFT_Detector_OT)
OFF	OFF
MOVING_SUPERSAFE	MOVING_SUPERSAFE
RESTORING_OFF	RESTORING_OFF
SUPERSAFE	SUPERSAFE
MOVING_SAFE	MOVING_SAFE
RESTORING_SUPERSAFE	RESTORING_SUPERSAFE
SAFE	SAFE
MOVING_STANDBY	MOVING_STANDBY
RESTORING_SAFE	RESTORING_SAFE
STANDBY	STANDBY
MOVING_READY	MOVING_READY
READY	READY
WARNING_RU	WARNING_RU
WARNING_Ladder	WARNING_Ladder
WARNING_PSU	WARNING_PSU
ERROR_RU	ERROR_RU
ERROR_Latchup	ERROR_Latchup
ERROR_Ladder	ERROR_Ladder
ERROR_PSU	ERROR_PSU
ERROR_Unexpected	ERROR_Unexpected

FIGURE B.20: The synchronization table for half

MFT_DET_H0D0 (MFT_Detector_OT)	MFT_DET_H0D0F0 (MFT_HP_OT)
OFF	OFF
MOVING_SAFE	MOVING_SAFE
RESTORING_OFF	RESTORING_OFF
SUPERSAFE	SUPERSAFE
MOVING_SAFE	MOVING_SAFE
RESTORING_SUPERSAFE	RESTORING_SUPERSAFE
SAFE	SAFE
MOVING_STANDBY	MOVING_STANDBY
RESTORING_SAFE	RESTORING_SAFE
STANDBY	STANDBY
MOVING_READY	MOVING_READY
READY	READY
WARNING_RU	WARNING_RU
WARNING_Ladder	WARNING_Ladder
WARNING_PSU	WARNING_PSU
ERROR_RU	ERROR_RU
ERROR_Latchup	ERROR_Latchup
ERROR_Ladder	ERROR_Ladder
ERROR_PSU	ERROR_PSU
ERROR_Unexpected	ERROR_Unexpected

FIGURE B.21: The synchronization table for disk

B.7 Face node

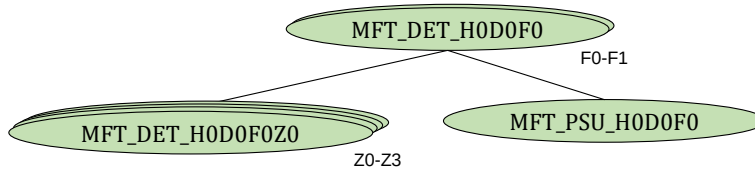


FIGURE B.22: The sub-tree structure of face

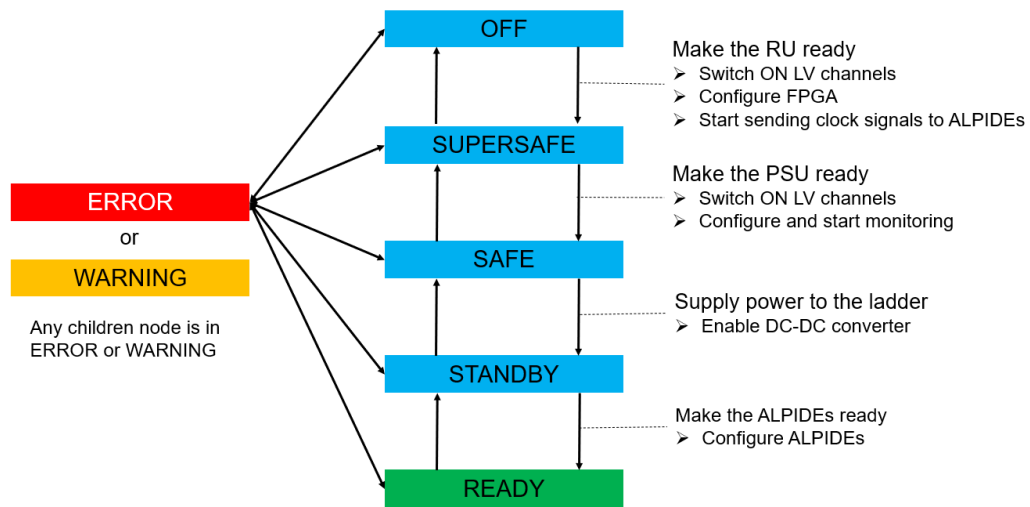


FIGURE B.23: The state diagram for face

MFT_DET_H0D0F0 (MFT_HP_OT)	MFT_DET_H0D0F0Z0 (MFT_ZONE_OT)	MFT_PSU_H0D0F0 (MFT_PSU_OT)
OFF	OFF	OFF
MOVING_SAFE	MOVING_RU_READY	OFF
RESTORING_OFF	RESTORING_OFF	OFF
SUPERSAFE	RU_READY	OFF
MOVING_SAFE	RU_READY	MOVING_STANDBY
RESTORING_SUPERSAFE	RU_READY	RESTORING_OFF
SAFE	RU_READY	STANDBY
MOVING_STANDBY	RU_READY→STANDBY	MOVING_ON
RESTORING_SAFE	STANDBY→RU_READY	RESTORING_STANDBY
STANDBY	STANDBY	ON
MOVING_READY	MOVING_READY	ON
READY	READY	ON
WARNING_RU	WARNING_RU	ANY
WARNING_Ladder	WARNING_Ladder	ANY
WARNING_PSU	ANY	WARNING
ERROR_RU	ERROR_RU	ANY
ERROR_Latchup	ERROR_Latchup	ANY
ERROR_Ladder	ERROR_Ladder	ANY
ERROR_PSU	ANY	ERROR
ERROR_Unexpected	ERROR_Unexpected	ANY
UNEXPECTED STATE		

FIGURE B.24: The synchronization table for face

B.8 PSU node

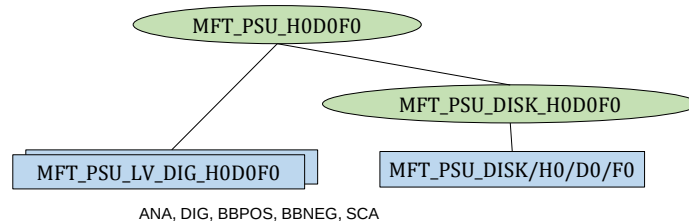


FIGURE B.25: The sub-tree structure of PSU

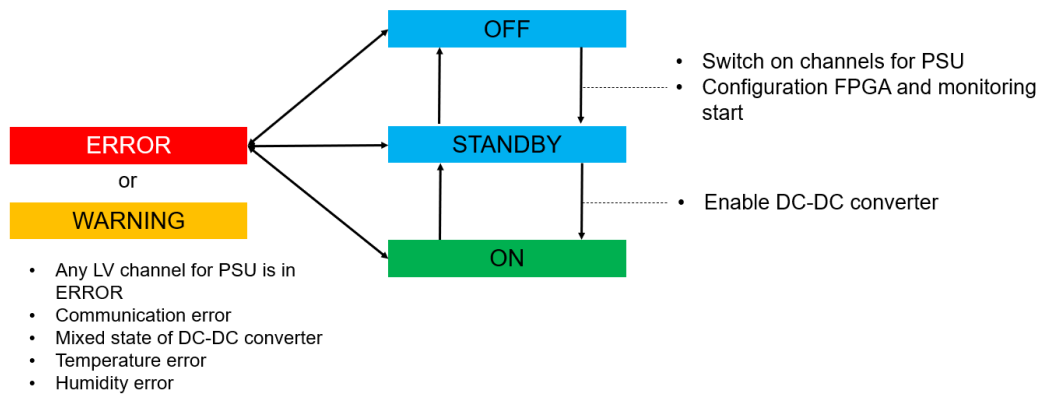


FIGURE B.26: The state diagram for PSU

MFT_PSU_H0D0F0 (MFT_PSU_OT)	MFT_PSU_LV_ANA_H0D0F0 (FwCaenChannel)	MFT_PSU_DISK_H0D0F0 (MFT_PSU_DISK_OT)
OFF	OFF	OFF
RESTORING_OFF	ON	OFF
MOVING_STANDBY	ON→OFF	RESTORING_OFF
STANDBY	OFF→ON	MOVING_STANDBY
RESTORING_STANDBY	ON	STANDBY
MOVING_ON	ON	RESTORING_STANDBY
ON	ON	MOVING_ON
WARNING	ANY	ON
ERROR	ANY	WARNING
	ERROR	ANY
	ANY	ERROR

FIGURE B.27: The synchronization table for PSU

MFT_PSU_DISK_H0D0F0 (MFT_PSU_DISK_OT)	MFT_PSU_TEMP_H0F0 (MFT_PSUDisk)
OFF	OFF
RESTORING_OFF	STANDBY→OFF
MOVING_STANDBY	OFF→STANDBY
STANDBY	STANDBY
MOVING_ON	STANDBY→ON
WARNING	WARNING
ON	ON
ERROR	ERROR

FIGURE B.28: The synchronization table for PSU disk

B.9 Zone node

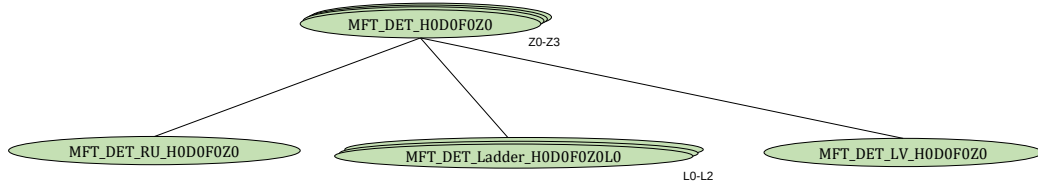


FIGURE B.29: The sub-tree structure of zone

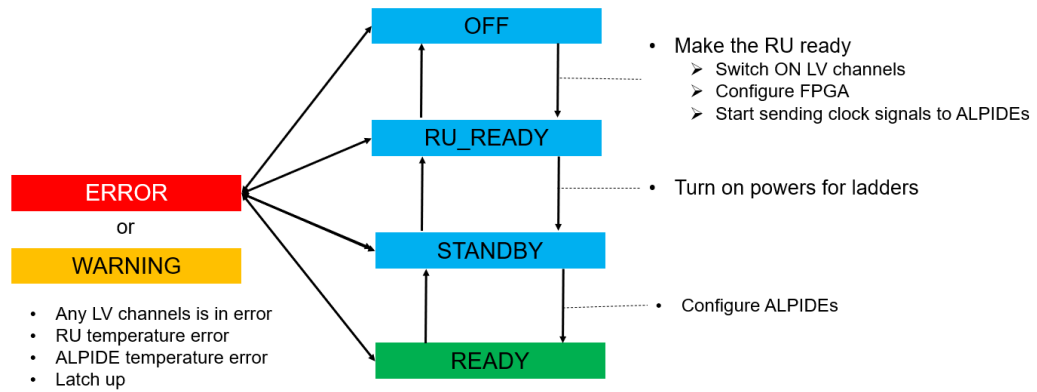


FIGURE B.30: The state diagram for zone

MFT_DET_HOD0FOZ0 (MFT_ZONE_OT)	MFT_DET_RU_HOD0FOZ0 (MFT_RU_OT)	MFT_DET_LV_HOD0FOZ0 (MFT_PSU_ZONE_OT)	MFT_FEE_HOD0FOZ0L0 MFT_Ladder_OT
OFF	OFF	OFF	NOT_READY
	MOVING_STANDBY		
	STANDBY		
	MOVING_CONFIGURED		
CONFIGURED			
MOVING_RU_READY	MOVING_RU_READY	OFF	NOT_READY
RESTORING_OFF	RESTORING_OFF	OFF	NOT_READY
RU_READY	READY	OFF	NOT_READY
STANDBY	READY	ON	NOT_READY
MOVING_READY	READY	ON	NOT_READY→READY
READY	READY	ON	READY
WARNING_RU	WARNING		ANY
WARNING_Ladder	ANY	ANY	WARNING
ERROR_RU	ERROR	ANY	ANY
ERROR_Latchup	ANY	ERROR	ANY
ERROR_Ladder	ANY	ANY	ERROR
ERROR_Unexpected		NOT DEFINED	

FIGURE B.31: The synchronization table for zone

B.10 RU node

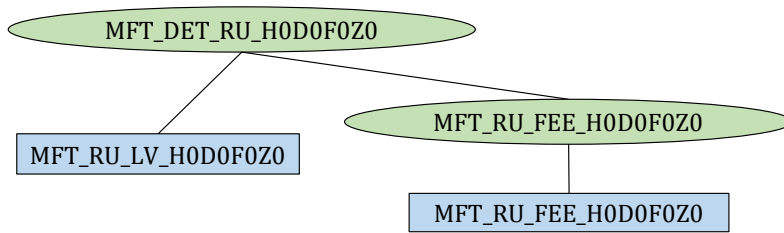


FIGURE B.32: The sub-tree structure of RU

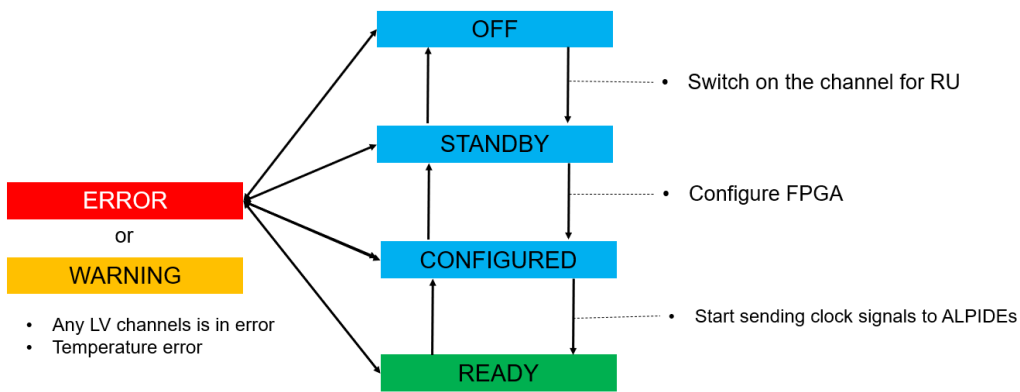


FIGURE B.33: The state diagram for RU

MFT_DET_RU_H0D0F0Z0 (MFT_RU_OT)	MFT_RU_LV_H0D0F0Z0 (FwCaenChannel)	MFT_DET_RU_H0D0F0Z0 (MFT_RU_FEE_OT)
OFF	OFF	NOT_READY
RESTORING_OFF	ON→OFF	NOT_READY
MOVING_STANBY	OFF→ON	NOT_READY
STANDBY	ON	NOT_READY
MOVING_CONFIGURED	ON	NOT_READY→CONFIGURED
CONFIGURED	ON	CONFIGURED
MOVING_READY	ON	CONFIGURED→READY
READY	ON	READY
WARNING	ANY	WARNING
ERROR	ERROR	ANY
	TRIPPED	ANY
	ANY	TOO_HOT
UNEXPECTED STATE		

FIGURE B.34: The synchronization table for RU

Appendix C

Operation Panels

GUI panels are developed for each devices on WinCC OA. It is described on Sec. 2.7. The standard user panels and the expert panels are as follows. The area surrounded by a red frame is a control that is only available in the expert panel.

C.1 Top MFT

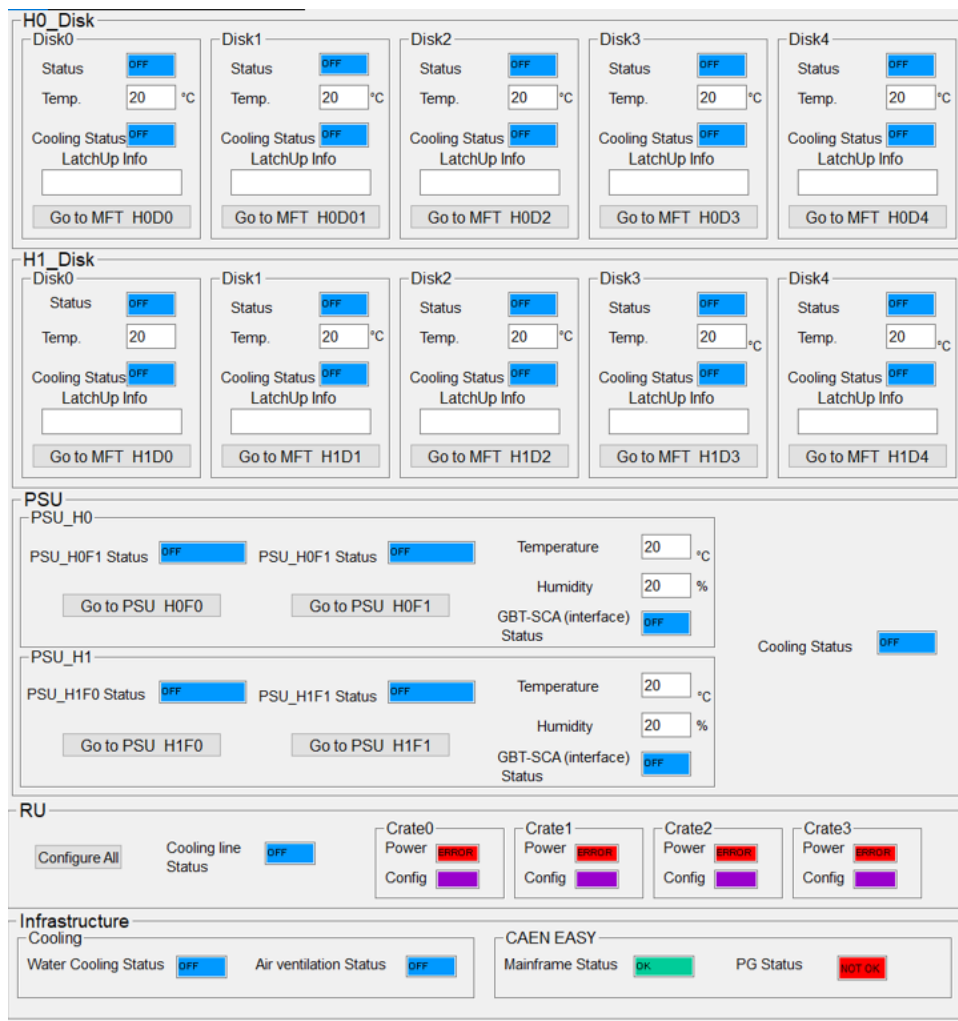


FIGURE C.1: The standard user panel for top MFT node



FIGURE C.2: The expert panel for top MFT node

C.2 Infrastructure



FIGURE C.3: The standard user panel for infrastructure node



FIGURE C.4: The expert panel for infrastructure node

C.3 Half MFT



FIGURE C.5: The standard user panel for half node



FIGURE C.6: The expert panel for half node

C.4 Disk



FIGURE C.7: The standard user panel for disk node



FIGURE C.8: The expert panel for disk node

C.5 Zone

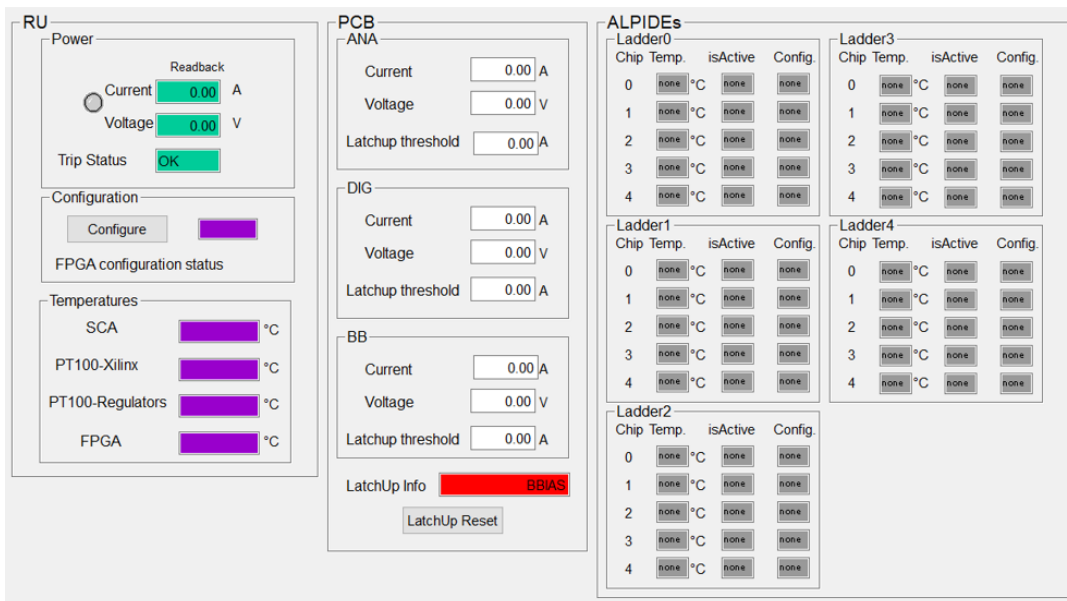


FIGURE C.9: The standard user panel for zone node

The image shows a complex control interface for a zone node, divided into several sections: RU (Rack Unit), PCB (Printed Circuit Board), and ALPIDEs. Red boxes and arrows highlight specific areas for parameter setting.

RU (Rack Unit) Section:

- Power:** Includes a power switch (ON/OFF), current (0.00 A), and voltage (0.00 V) readbacks. A red box highlights the "Advanced Settings" and "Configuration" tabs, with an arrow pointing to the text "Set Parameters for RU".
- Temperatures:** Displays SCA, PT100-Xilinx, PT100-Regulators, and FPGA temperatures.
- Configuration:** Includes "FPGA configuration status" and "Advanced Settings" (highlighted with a red box).

PCB (Printed Circuit Board) Section:

- ANA and DIG Switches:** Includes "ANA and DIG Switch" (ON/OFF) and "BB Switch" (ON/OFF).
- Latchup Info:** Includes "Latchup Reset" and "Advanced Settings" (highlighted with a red box).

ALPIDEs Section:

- Contains four ladder sections (Ladder0, Ladder1, Ladder2, Ladder3, Ladder4), each with a table of chip temperatures and status indicators. A red box highlights the "Advanced Settings" button for each ladder, with an arrow pointing to the text "Set Parameters for each ALPIDE".

Parameter Setting Panels:

- Top Right Panel:** A grid of parameter settings for various registers, including REG_VCASN, REG_MODECONTROL, REG_VRESETD, REG_VCASN2, REG_FROM_CONFIG1-3, REG_VPULSEH, REG_VPULSEL, REG_FROM_PULSING1-2, REG_VCLIP, REG_FROM_PULSING2, REG_IBIAS, REG_CMUDMU_CONFIG, REG_DTU_CONFIG, and REG_DTU_DACS. A "Set" button is at the bottom.
- Bottom Right Panel:** A smaller grid of parameter settings for REG_MODECONTROL, REG_VRESETD, REG_VCASP, REG_VPULSEH, REG_VPULSEL, REG_VCLIP, REG_IBIAS, REG_CMUDMU_CONFIG, REG_VBIAS, REG_DTU_CONFIG, REG_VCASP, and REG_DTU_DACS. A "Set" button is at the bottom.
- Bottom Left Panel:** A panel for setting "ANA", "DIG", and "BB" latchup thresholds and voltage settings, each with a "Set" button.

FIGURE C.10: The expert panel for zone node

C.6 RU



FIGURE C.11: The standard user panel for RU node



FIGURE C.12: The expert panel for RU node

PSU_H0D0F0

Cooling

Input Water Pressure: 120 bar Water Flow: 20 Valve Status: 20 Input Water Temp.: 20 °C Output Water Temp.: 20 °C

PSU Mezzanin Temp. 1: 20 °C PSU Mezzanin Temp. 2: 20 °C PSU Humidity: 20 %

Output Power to Zone

Zone0	Zone1	Zone2	Zone3
ANA Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	ANA Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	ANA Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	ANA Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A
DIG Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	DIG Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	DIG Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	DIG Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A
BB Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	BB Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	BB Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A	BB Current: <input type="text"/> A Voltage: <input type="text"/> V Latching threshold: <input type="text"/> A
LatchingUp Info <input type="text"/> LatchingUp Reset	LatchingUp Info <input type="text"/> LatchingUp Reset	LatchingUp Info <input type="text"/> LatchingUp Reset	LatchingUp Info <input type="text"/> LatchingUp Reset
GBT-SCA Comm. Status <input type="checkbox"/>	DC-DC Converter Zone0/1 Status <input type="checkbox"/>	DC-DC Converter Zone2/3 Status <input type="checkbox"/>	

FIGURE C.13: The standard user panel for psu node

PSU_H0D0F0

Cooling

Input Water Pressure: 120 bar Water Flow: 20 Valve Status: 20 Input Water Temp.: 20 °C Output Water Temp.: 20 °C

PSU Mezzanin Temp. 1: 20 °C PSU Mezzanin Temp. 2: 20 °C PSU Humidity: 20 %

Output Power to Zone

Zone	ANA	DIG	BB	ANA and DIG ON/OFF	BB ON/OFF	LatchUp Info
Zone0	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	ON OFF	ON OFF	LatchUp Reset Advanced Settings
Zone1	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	ON OFF	ON OFF	LatchUp Reset Advanced Settings
Zone2	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	ON OFF	ON OFF	LatchUp Reset Advanced Settings
Zone3	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	Current: [] A Voltage: [] V Latchup threshold: [] A	ON OFF	ON OFF	LatchUp Reset Advanced Settings

GBT-SCA DC-DC Converter Zone0/1 DC-DC Converter Zone2/3

Comm. Status: [] Status: [] Status: []

Configuration Enable/Disable Enable/Disable

ANA and DIG: Switch ON all Switch OFF all BB: Switch ON all Switch OFF all

FIGURE C.14: The expert panel for psu node

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